P21302

256x64 Yellow OLED

Application Notes

Revision History

Version	Content
X01	First release

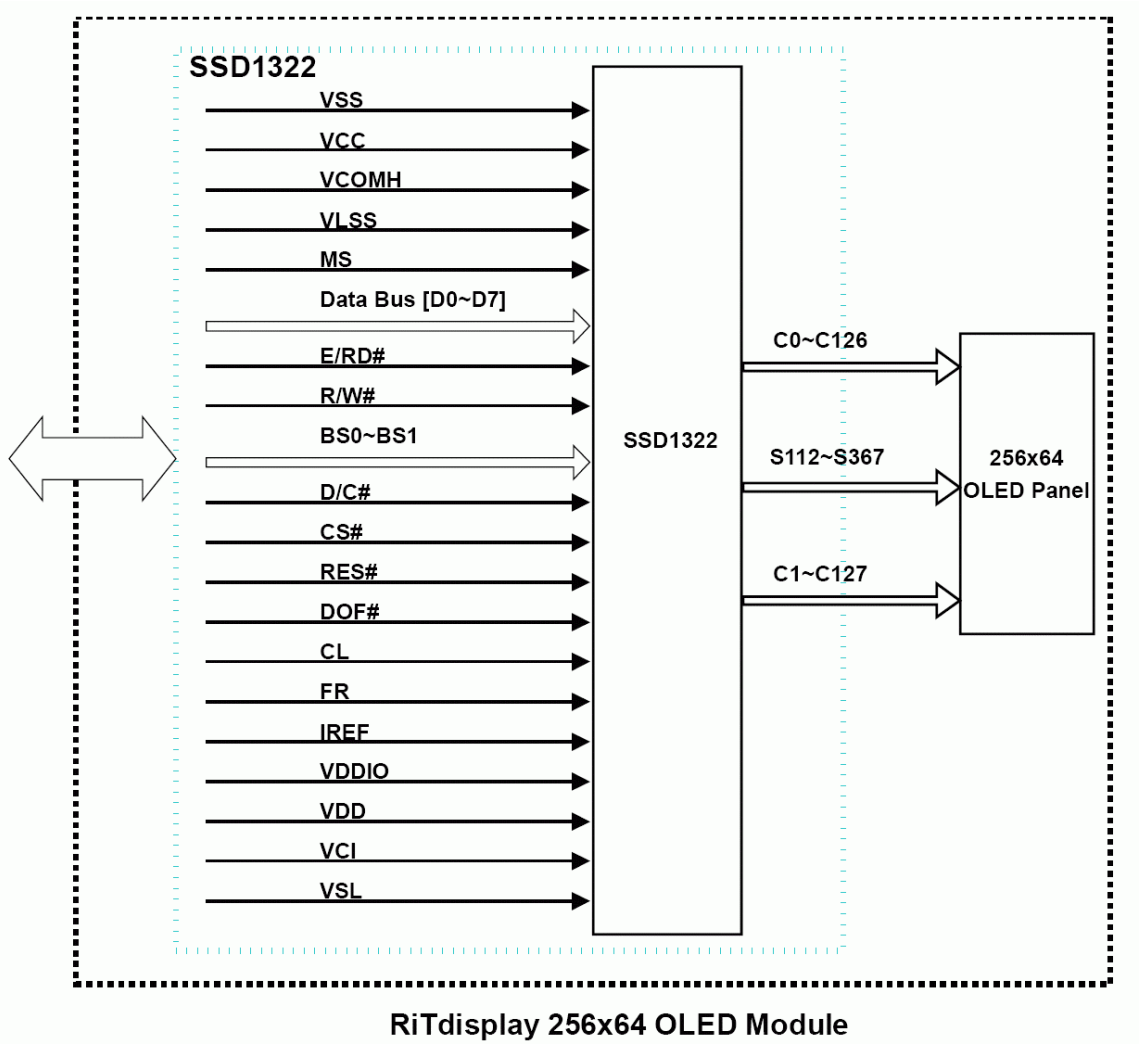
DESCRIPTION

P21302 is 256x64 passive OLED module with controller for many compact portable applications.

FEATURE

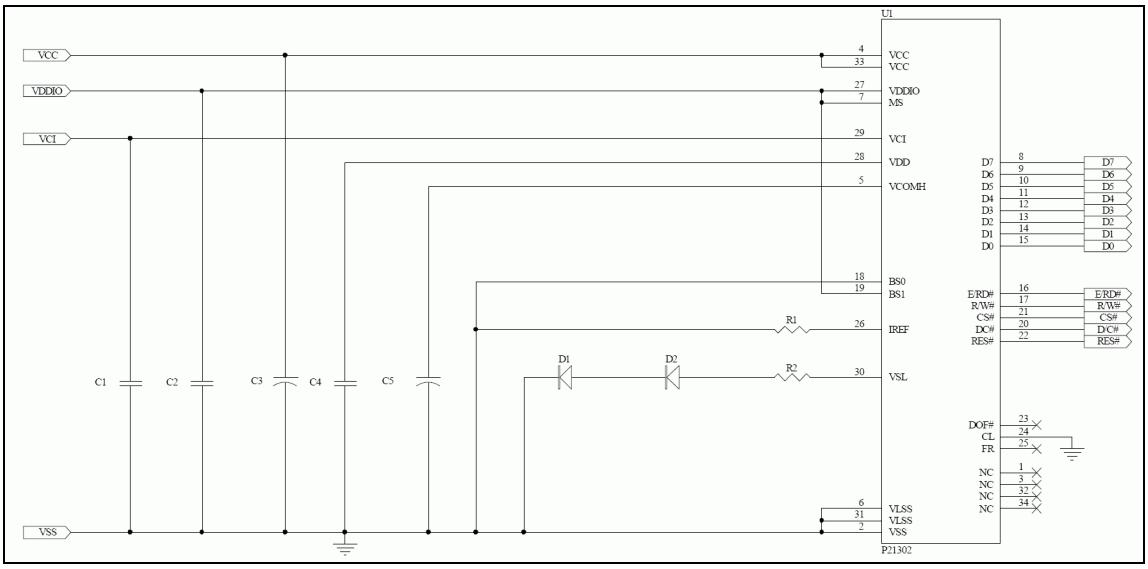
- Panel matrix 256x64.
- Driver IC: SSD1322.
- VCC =14.5V
- VCI =2.4V~3.5V
- VDDIO =1.65V~ VCI
- 16 gray scale levels supported by embedded 480 x 128 x 4 bit SRAM display buffer.
- 8-bit 6800/8080-series parallel interface, 3/4-wire Serial Peripheral Interface.

FUNCTION BLOCK DIAGRAM



RiTdisplay 256x64 OLED Module

Application circuit



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

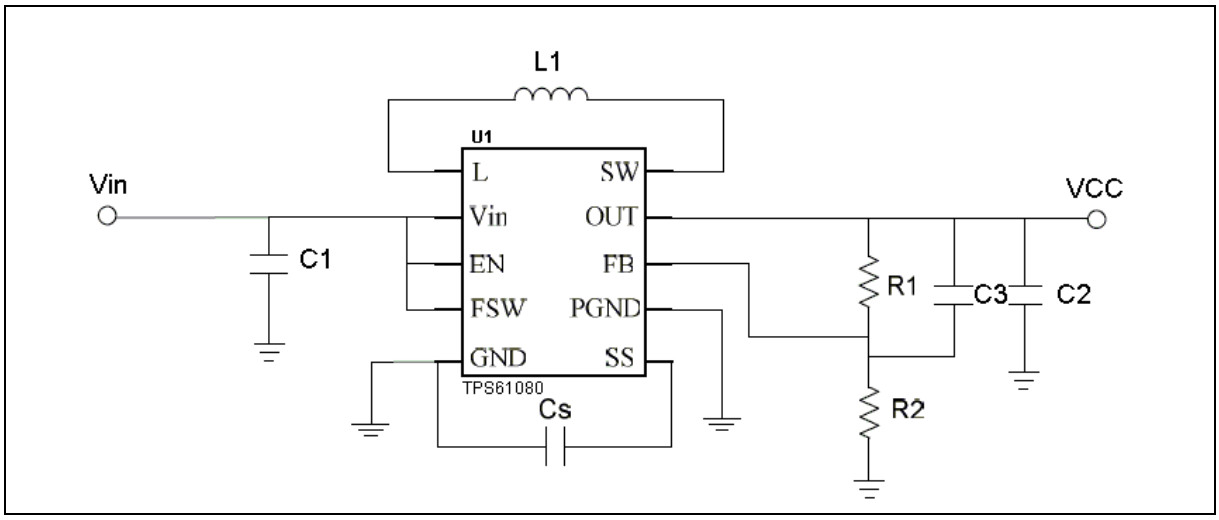
R1: 430K ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 8bits interface.

DC-DC application circuit for OLED module



Recommend components:

The C1: 4.7uF/6.3V.

The C2: 4.7 uF/35V Tantalum type capacitor.

The C3: 50pF/16V.

The Cs: 47nF/16V.

The R1: 1.2M ohm/ 1%.

The R2: 110K ohm/ 1%.

The L1: 10uH.

The U1: TPS61080

The R1, R2 and C3 value should be fine tune by customer.

PIN ASSIGNMENT

PIN NAME	PIN NO.	DESCRIPTION
NC	1	No connection.
VSS	2	Ground pin.
NC	3	No connection.
VCC	4	Power supply for panel driving voltage.
VCOMH	5	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
VLSS	6	Analog system ground pin.
MS	7	This pin must be connected to VDDIO to enable the chip.
D7	8	These pins are bi-directional data bus connecting to the MCU data bus.
D6	9	
D5	10	
D4	11	
D3	12	
D2	13	
D1	14	
D0	15	
E/RD#	16	When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal.Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.
R/W#	17	When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to VSS.
BS0	18	MCU bus interface selection pins.
BS1	19	
DC#	20	This pin is Data/Command control pin connecting to the MCU.
CS#	21	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.
RES#	22	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.
DOF#	23	This pin is No Connection pins.
CL	24	External clock input pin.
FR	25	This pin is No Connection pins.
IREF	26	A resistor should be connected between this pin and VSS.
VDDIO	27	Power supply for interface logic level. It should be matched with the MCU interface voltage level.
VDD	28	Power supply pin for core logic operation. A capacitor is required to connect between this pin and VSS.

VCI	29	Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO.
VSL	30	This is segment voltage reference pin. When external VSL is used, connect with resistor and diode to ground.
VLSS	31	Analog system ground pin.
NC	32	No connection.
VCC	33	Power supply for panel driving voltage.
NC	34	No connection.

Application Initial Setting

```
void initial(void)
{
comm_out(0xae);        //Display OFF

comm_out(0xfd);        //Set Command Lock
data_out(0x12);

comm_out(0xa0);        //Set Re-map and Dual COM Line mode
data_out(0x04);
data_out(0x11);

comm_out(0xa1);        //Set Display Start Line
data_out(0x00);

comm_out(0xa2);        //Set Display Offset
data_out(0x00);

comm_out(0xa6);        //Normal Display

comm_out(0xab);        //Function Selection
data_out(0x01);        //Enable internal VDD regulator

comm_out(0xb1);        //Set Phase Length
data_out(0x8f);

comm_out(0xb3);        //Set Front Clock Divider/Oscillator Frequency
data_out(0x91);

comm_out(0xb4);        //Enable external VSL
data_out(0xa0);
data_out(0xfd);

comm_out(0xb6);        //Set Second Precharge Period
data_out(0x08);

comm_out(0xb9);        //Select Default Linear Gray Scale table
```

```
comm_out(0xbb);       //Set Pre-charge voltage
data_out(0x1f);

comm_out(0xbe);       //Set VCOMH
data_out(0x07);

comm_out(0xc1);       //Set Contrast Current
data_out(0x58);

comm_out(0xc7);       //Master Contrast Current Control
data_out(0x0f);

comm_out(0xca);       //Set MUX Ratio
data_out(0x3f);

comm_out(0xd1);       //Display Enhancement B
data_out(0x82);
data_out(0x20);

comm_out(0xaf);       //Display ON
}
```

/*After power on the OLED driver IC, please clean the DDRAM.*/

```
void CleanDDR(void)
{
int i,j;
comm_out(0x15);       //set column address
data_out(0x00);
data_out(0x77);
comm_out(0x75);       //set row address
data_out(0x00);
data_out(0x7f);
comm_out(0x5c);       //write RAM command
for(i=0;i<128;i++)
{
   for(j=0;j<240;j++)
```

```
   { data_out(0x00); }
}
}

void show_data(char a)
{
int i,j;
comm_out(0x15);       //set column address
data_out(0x1c);
data_out(0x5b);
comm_out(0x75);       //set row address
data_out(0x00);
data_out(0x3f);
comm_out(0x5c);       //write RAM command
for(i=0;i<64;i++)
 {
   for(j=0;j<128;j++)
   {
     data_out(a);
   }
 }
}
```

GRAPHIC DISPLAY DATA RAM(GDDRAM)

The GDDRAM address map shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel.

For example D30480[3:0] corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D30717, D30718, D30719 represent the 480x128 data nibbles in the GDDRAM.

GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG476	SEG477	SEG478	SEG479	SEG Outputs
		00		00			77		77		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	01	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]		D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
|	|									
COM126	7E	D30241[3:0]	D30241[7:4]	D30240[3:0]	D30240[7:4]		D30479[3:0]	D30479[7:4]	D30478[3:0]	D30478[7:4]	
COM127	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]		D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

POWER ON/OFF SEQUENCE

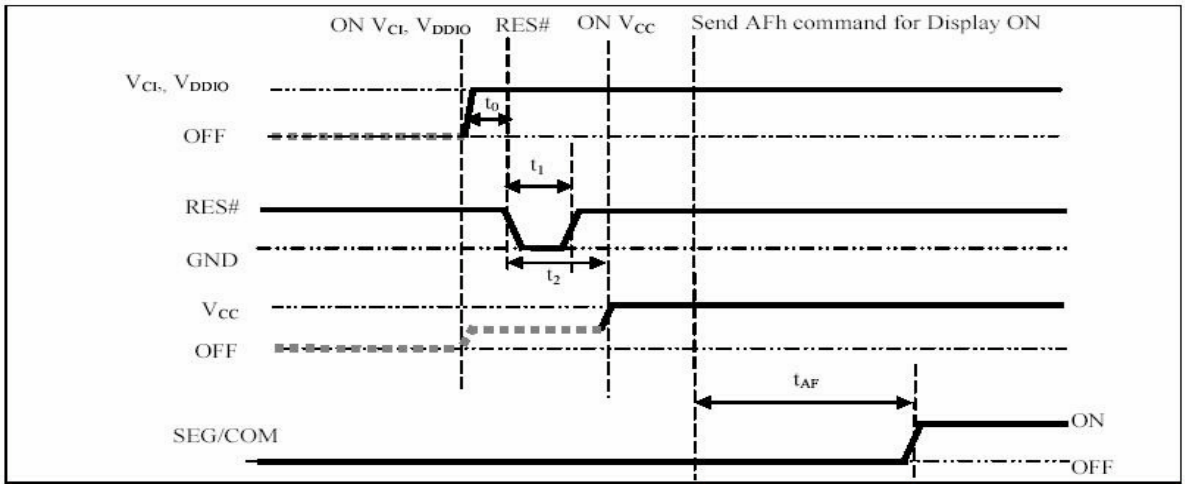
***Power ON sequence**:*

1.Power ON V_{CI},V_{DDIO}.

2.After V_{CI},V_{DDIO} become stable,set wait time at least 1ms (t_0) for internal V_{DD} become stable.Then set RES# pin LOW (logic low) for at least 100us (t1)[4] and then HIGH (logic high).

3.After set RES# pin LOW (logic low), wait for at least 100us(t_2).
Then Power ON V_{CC}.[1]

4.After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

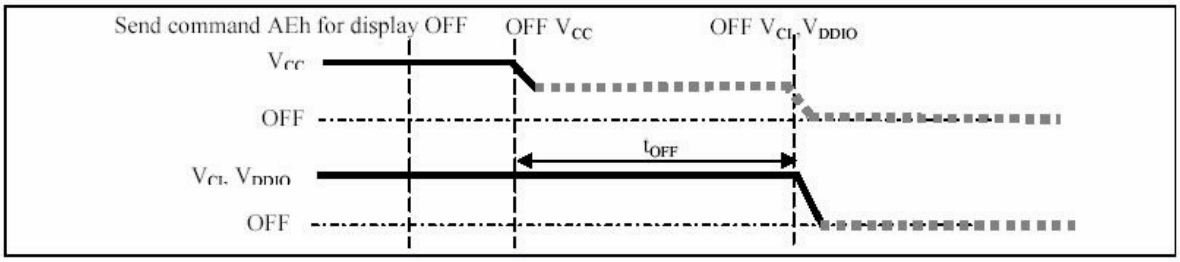


Power OFF sequence:

1.Send command AEh for display OFF.

2.Power OFF V_{CC}. [1], [2]

3.Wait for t_{OFF}. Power OFF V_{CI},V_{DDIO}.
(where Minimum t_{OFF}=80ms[3], Typical t_{OFF}=100ms)



Note:

(1).Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure.

(2).V_{CC} should be kept float (disable) when it is OFF.

(3).V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

(4).The register values are reset after t_1.

(5).Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

Thank You