P19301
128x64 OLED Application Notes
(I^2C)

Revision History

Version	Content
X01	First release

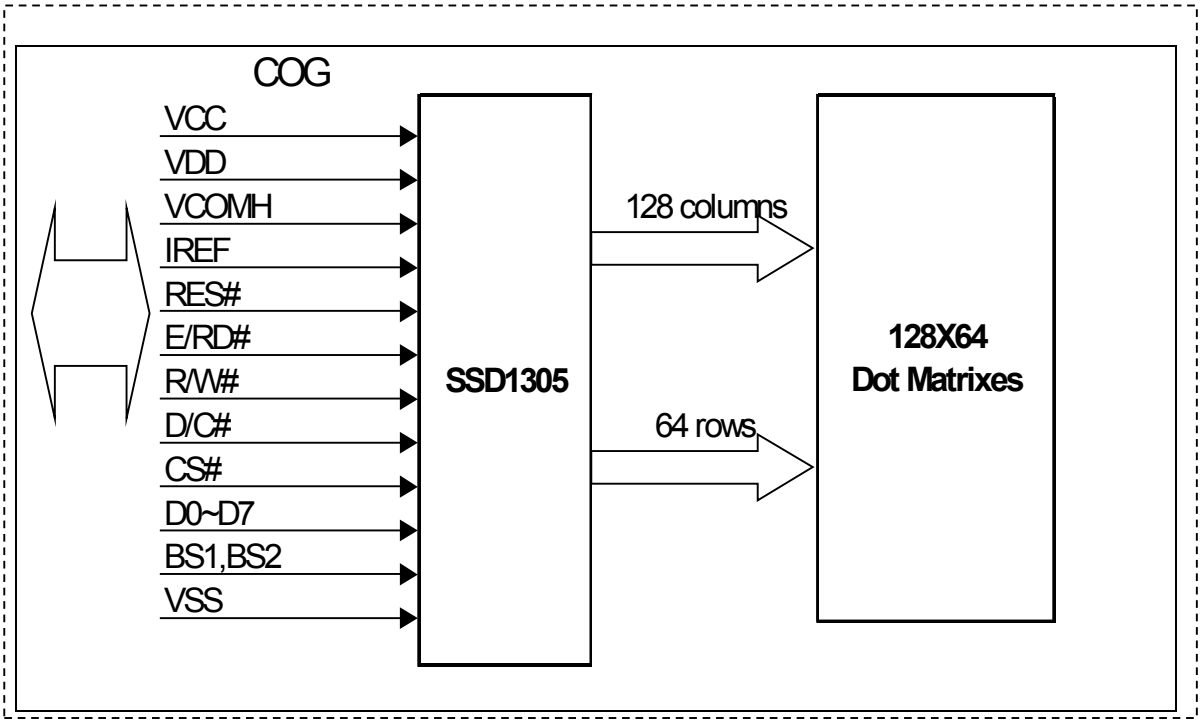
DESCRIPTION

This is a 128X64 dot matrix passive OLED module with controller for many compact portable applications.

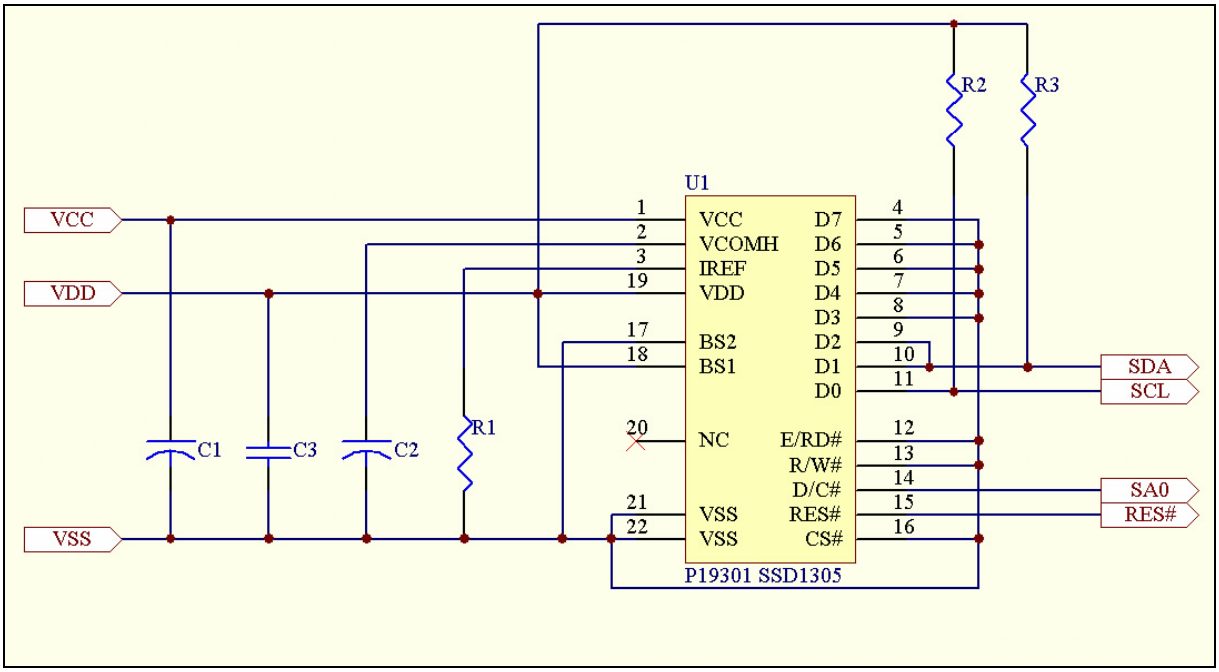
FEATURE

- VCC=15V
- VDD=2.4V~3.5V
- Color: Yellow
- Panel resolution: 128*64
- Driver IC: SSD1305
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface, I^2C interface.
- Display data RAM: 132X64 = 8448 bits.
- 256 steps contrast current control.
- Internal oscillator.
- Adjustable frame frequency.

FUNCTION BLOCK DIAGRAM



APPLICATION CIRCUIT



Recommend component:

The C1: 4.7uF/35V Tantalum type or VISHAY (572D475X0025A2T)

The C2: 4.7uF/35V Tantalum type or VISHAY (572D475X0025A2T)

The C3: 0.1uF/6.3V.

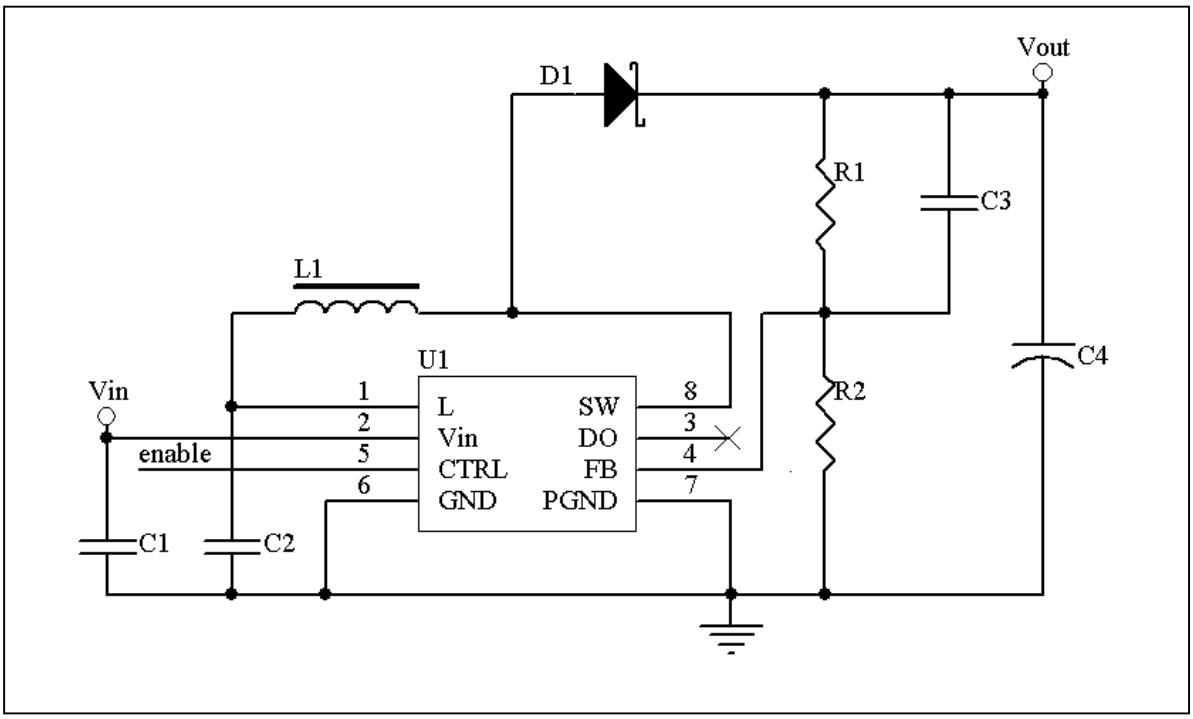
The R1: 1M ohm/ 1%.

The R2, R3: 10K ohm/ 5%

The U1: P19301 OLED module

The R2, R3 value should be fine tune by customer.

External DC-DC application circuit



Recommend component:

The C1: 0.1uF/6.3V.

The C2: 4.7 uF/6.3V.

The C3: 10pF/16V.

The C4: 4.7 uF/35V Tantalum type capacitor.

The R1: 1M ohm/ 1%.

The R2: 91K ohm/ 1%.

The D1: SCHOTTY DIODE.

The L1: 22uH.

The U1: HPA00483DRBR

The R1, R2 and C3 value should be fine tune by customer.

Note: a. The HPA00483DRBR is low cost DC/DC for TI.

b. The HPA00483DRBR spec is same as TPS61045.

PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VCC	1	Power supply for analog circuit.
VCOMH	2	Com Voltage Output. A capacitor should be connected between this pin and VSS.
IREF	3	Reference current input pin. A resistor should be connected between this pin and VSS.
D7	4	In I^2C mode, tie to low.
D6	5	
D5	6	
D4	7	
D3	8	
D2	9	I^2C serial data pin. In I^2C mode, D2, D1 should be tied together and serve as SDA.
D1	10	
D0	11	SCL. I^2C serial clock pin.
E/RD#	12	In I^2C mode, tie to low.
R/W#	13	In I^2C mode, tie to low.
D/C#	14	In I^2C mode, this pin acts as SA0 for slave address selection.
RES#	15	Reset signal input. When it's low, initialization of SSD1305 is executed.
CS#	16	In I^2C mode, tie to low.
BS2	17	Interface select pin. In I^2C mode, tie to low.
BS1	18	Interface select pin. In I^2C mode, tie to high.
VDD	19	Power supply for logic circuit.
NC	20	No connection.
VSS	21	Ground.
VSS	22	Ground.

Initial software

```
/*
1. The slave address is either “b0111100” or “b0111101” by changing the SA0
to LOW or HIGH (D/C pin acts as SA0).
2. The control byte is definition of command or data.
*/
void init_SSD1305(void)
{
comm_out(0xad); //set dc-dc off
comm_out(0x8e);
comm_out(0xae); //set display off
comm_out(0xa8); //set multiplex ratio
comm_out(0x3f); //64MUX
comm_out(0xd3); //set display offset
comm_out(0x00); //second byte
comm_out(0xda); //set com pins hardware
comm_out(0x12); //second byte
comm_out(0x40); //set display start line
comm_out(0xa0); //set segment re-map
comm_out(0xc0); //set COM output scan direction
comm_out(0xa6); //set normal/inverse display
comm_out(0xa4); //set entire display
comm_out(0x81); //set contrast control
comm_out(0xA7); //second byte
comm_out(0xd9); //Set Pre-charge Period
comm_out(0xf1); //
comm_out(0xd5); //set display clock divide ratio/oscillator frequency.
comm_out(0xc0); //second byte
comm_out(0xd8); //set area colour mode/low power display mode
comm_out(0x05); //second byte
comm_out(0xaf); //set display on
}

void set_display_on(void)
{
while(!VCC_stable); //waiting until VCC is stable
```

```
comm_out(0xaf);     //set display on
}

void show_data(data char a)
{
int i,j;
for(i=0;i<8;i++){
  comm_out(0xb0+i);
  comm_out(0x00);
  comm_out(0x10);
  for (j=0;j<128;j++)
    data_out(a);
  }
}
```

MCU I²C INTERFACE

1) The master device initiates the data communication by a start condition.

2) The slave address is following the start condition for recognition use. For the SSD1305, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).

3) The write mode is established by setting the R/W# bit to logic "0".

4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.

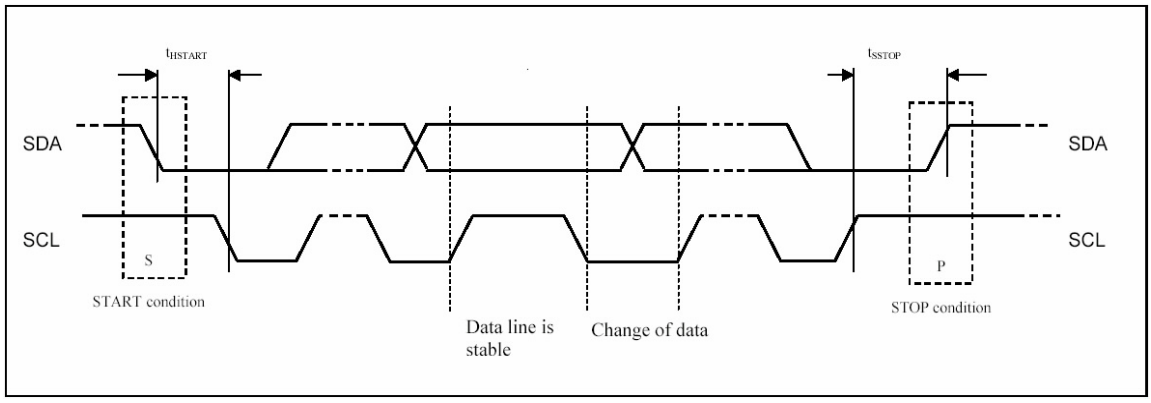
a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.

b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

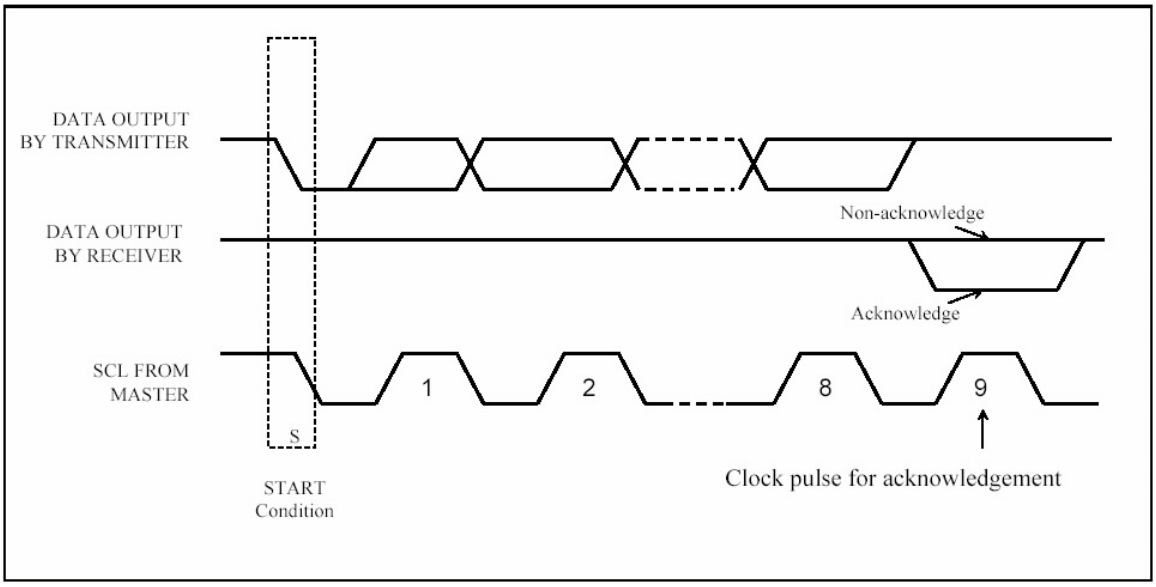
6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

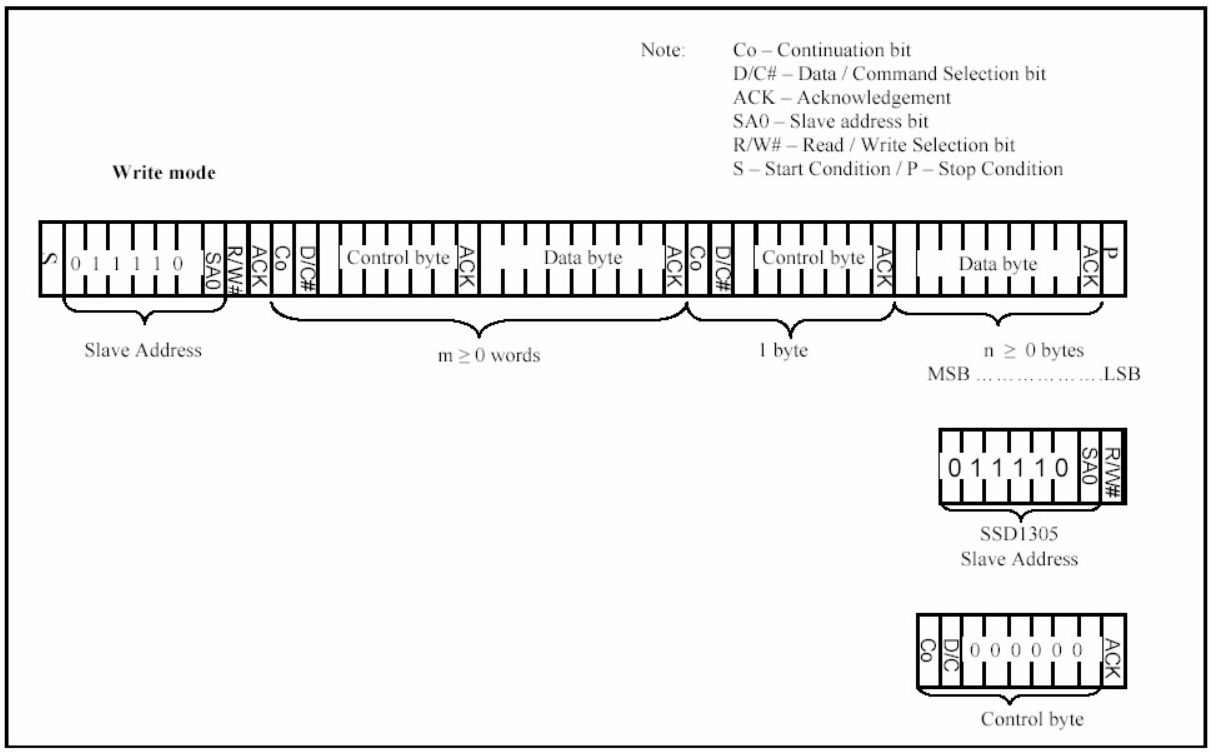
Definition of Start/Stop and Data Transfer Condition



Definition of the acknowledgement condition



I²C-bus data format



Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed.
The size of the RAM is 132x64= 8448bits.
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

OUT	Row Address Direction='1'	Row Address Direction='0'		Column Address Remap='0'	Column Address Remap='1'	OUT
				0x00h	0x83h	SEG0
				0x01h	0x82h	SEG1
				0x02h	0x81h	SEG2
				0x03h	0x80h	SEG3
				0x04h	0x7Fh	SEG4
				0x05h	0x7Eh	SEG5
				0x06h	0x7Dh	SEG6
				0x07h	0x7Ch	SEG7
				...		
				0x80h	0x03h	SEG128
				0x81h	0x02h	SEG129
				0x82h	0x01h	SEG130
				0x83h	0x00h	SEG131
COM0	0x3Fh	0x00h	PAGE 0	D0		
COM1	0x3Eh	0x01h		D1		
COM2	0x3Dh	0x02h		D2		
COM3	0x3Ch	0x03h		D3		
COM4	0x3Bh	0x04h		D4		
COM5	0x3Ah	0x05h		D5		
COM6	0x39h	0x06h		D6		
COM7	0x38h	0x07h		D7		
COM8	0x37h	0x08h	PAGE 1	D0		
COM9	0x36h	0x09h		D1		
COM10	0x35h	0x0Ah		D2		
COM11	0x34h	0x0Bh		D3		
COM12	0x33h	0x0Ch		D4		
COM13	0x32h	0x0Dh		D5		
COM14	0x31h	0x0Eh		D6		
COM15	0x30h	0x0Fh		D7		
COM16	0x2Fh	0x10h	PAGE 2	D0		
COM17	0x2Eh	0x11h		D1		
COM18	0x2Dh	0x12h		D2		
COM19	0x2Ch	0x13h		D3		
COM20	0x2Bh	0x14h		D4		
COM21	0x2Ah	0x15h		D5		
COM22	0x29h	0x16h		D6		
COM23	0x28h	0x17h		D7		
⋮						
COM48	0x0Fh	0x30h	PAGE 6	D0		
COM49	0x0Eh	0x31h		D1		
COM50	0x0Dh	0x32h		D2		
COM51	0x0Ch	0x33h		D3		
COM52	0x0Bh	0x34h		D4		
COM53	0x0Ah	0x35h		D5		
COM54	0x09h	0x36h		D6		
COM55	0x08h	0x37h		D7		
COM56	0x07h	0x38h	PAGE 7	D0		
COM57	0x06h	0x39h		D1		
COM58	0x05h	0x3Ah		D2		
COM59	0x04h	0x3Bh		D3		
COM60	0x03h	0x3Ch		D4		
COM61	0x02h	0x3Dh		D5		
COM62	0x01h	0x3Eh		D6		
COM63	0x00h	0x3Fh		D7		

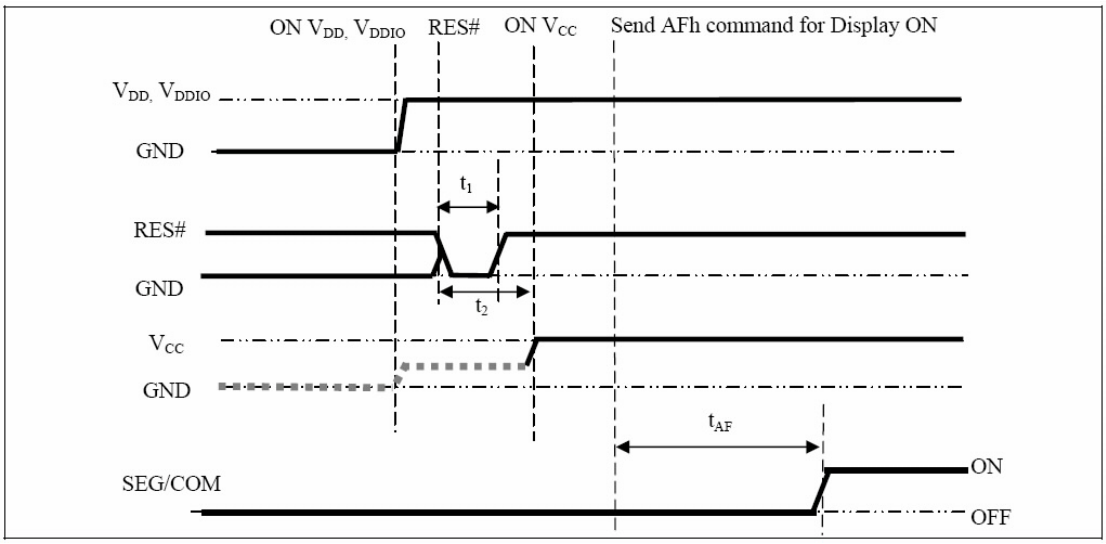
After initial the driver IC, user must clear the whole DDRAM.

```
void cleanDDR(void)
{
int i,j;
for(i=0;i<8;i++){
  comm_out(0xb0+i);
  comm_out(0x00);
  comm_out(0x10);
  for (j=0;j<132;j++)
    data_out(0x00);
  }
}
```

Power On/Off Sequence

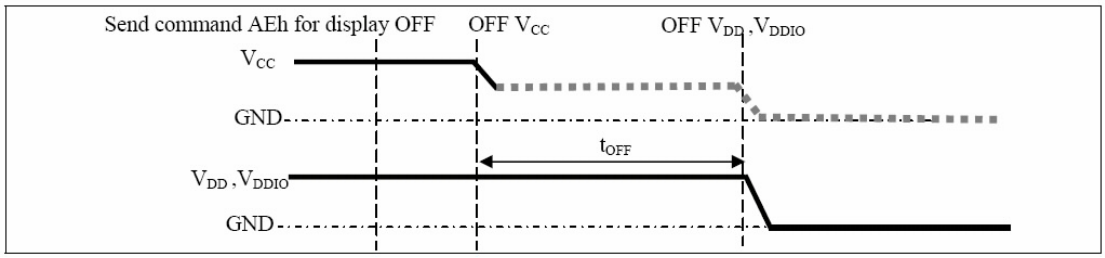
Power ON sequence:

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

THANK YOU