中显液晶
技术资料

中显COG玻璃使用说明书

ZX12864-13焊接式

2009年3月15日

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CONTENTS

1. MECHANICAL DATA

Item	Contents	Unit
LCD Mounting mode	COG LCD FPC	
LCD Display mode	Reflective, Transflective and positive	
LCD Display type	STN: Yellow Green mode, Gray mode, Blue mode	
	FSTN	
Viewing direction	6 O'clock or 12 O'clock	
LCD Module size	42.0(W)×31.0(H)×2.0(D, MAX)	mm
LCD Viewing area	38.0(W)×22.0(H)	mm
LCD Display format	128×64 dot matrix	
Dot size	0.25(W)×0.28(H)	mm
Dot pitch	0.28(W)×0.31(H)	mm
LCD Duty	1/64	
LCD Bias	1/9	
LCD Controller/driver LSI	NT7532 (COG)	
LCM Operation temperature (N*)	0~+50	℃
LCM Storage temperature (N*)	-10~+60	℃
LCM Operation temperature (E*)	-20~+70	℃
LCM Storage temperature (E*)	-30~+80	℃
Back light	Edge light LED: Green, White, Blue	
	EL: White, Yellow green, Blue	
Input data	8080 MPU Interface	
	6800 Series MPU Interface	
	Series data input	
	Parallel data input	
Power supply	2.4-5.0V single power input.	V
	Built- in DC/DC converter for LCD driving.	
	High-accuracy voltage adjustment circuit (thermal gradient –0.05%/℃)	
LCD Expected life	50,000	Hours

NOTICE:

LED*: LED Backlight
EL or None*: EL Backlight or no backlight
N*: Normal temperature type
E*: Extended temperature type

2. ABSOLUTE MAXIMUM RATINGS

2.1 ELECTRICAL ABSOLUTE RATINGS

V_{SS}=0V

Item	Symbol	Min	Max	Unit	Note
Power supply for logic	V_{DD}-V_{SS}	-0.3	7.0	V	
Power supply for LCD	V_{DD}-Vo	-0.3	12.0	V	
Input voltage	Vi	-0.3	Vdd+0.3	V	

2.2 ENVIRONMENTAL ABSOLUTE RATINGS

Item		Symbol	Min	Max	Unit
Normal type	Operating temperature	T0	0	+50	℃
	Storage temperature	Ts	-10	+60	℃
Wide type	Operating temperature	T0	-20	+70	℃
	Storage temperature	Ts	-30	+80	℃
Humidity		---	---	85	%RH

3.ELECTRRICAL CHARACTERISTICS

3.1 ELECTRRICAL CHARACTERISTICS

V_{SS}=0V

Item		Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	Logic	V_{DD}	----	2.4	3.0	5.0	V
	Booster output	V_{OUT}	----	6.0		12.0	V
	LCD drive	Vo	----	4.5	---	11.5	V
High-level input voltage		V_{IHC}	----	0.8V_{DD}	---	V_{DD}	V
Low- level input voltage		V_{ILC}	----	V_{SS}	---	0.2V_{DD}	V
High-level output voltage		V_{OHC}	I_{OH}=-0.5mA	0.8V_{DD}	---	V_{DD}	V
Low- level output voltage		V_{OLC}	I_{OL}=0.5mA	V_{SS}	---	0.2V_{DD}	V
Sleep mode		I_{SP}	25℃	---	0.01	5.0	μA
Standby mode		I_{SB}	25℃	---	4.0	8.0	μA

3.2 SPECIFICATION FOR LED BACKLIGHT

EDGE LED BACKLIGHT

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	3.2	3.4	3.6	
LED Consumption current	mA	40	60	80	
LED Color		Green			

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	3.2	3.4	3.6	
LED Consumption current	mA	40	60	80	
LED Color		White			

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	3.2	3.4	3.6	
LED Consumption current	mA	40	60	80	
LED Color			Blue		

3.3 SPECIFICATION FOR EL BACKLIGHT

Item	Unit	Min	Typ	Max	Condition
Supply voltage	V	---	100	125	
Supply frequeney	Hz	---	400	400	
Initial brightness	cd/m	40	---	--	AC 100Vrms,400Hz,Dark room
Current	mA	3.3_+30%			AC 100Vrms,400Hz,Dark room
Operating temperature	℃	-20~+50			
Storage temperature	℃	-20~+60			
Luminous color	--	White			AC 100Vrms,400Hz,Dark room
Life time	Hrs	3,000			Note 1

Note 1: Half value of initial brightness at 20℃ 60%RH

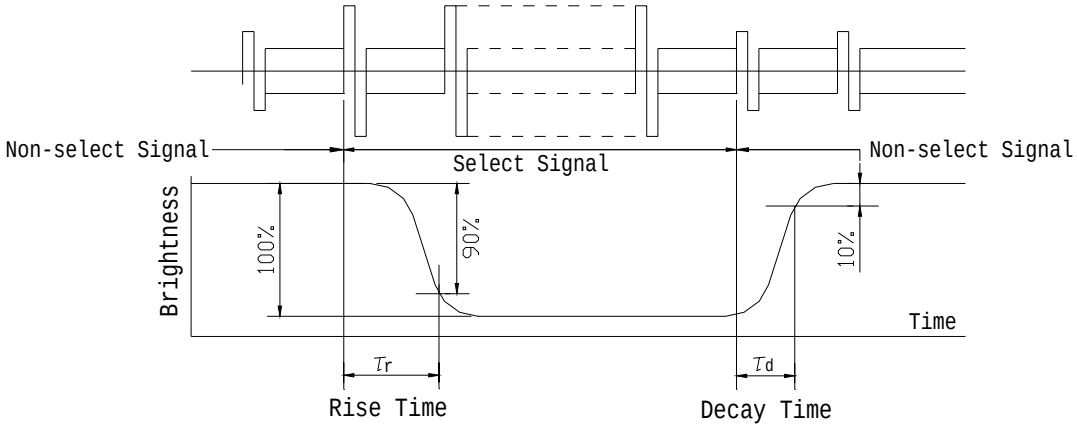
4. OPTICAL CHARACTERISTICS

STN TYPE Ta=25℃

Item	Symbol	Condition	Min	Typ	Max	Unit	Reference
Viewing angle	θ	K≧2.0 ϕ=0o	40o	---	---	deg	Note1,2
Contrast ration	K	θ=5o ϕ=0o	---	5	---	---	Note3
Response time(rise)	Tr	θ=5o ϕ=0o	---	110	165	ms	Note4
Response time(fall)	Tf	θ=5o ϕ=0o	---	110	165	ms	Note4

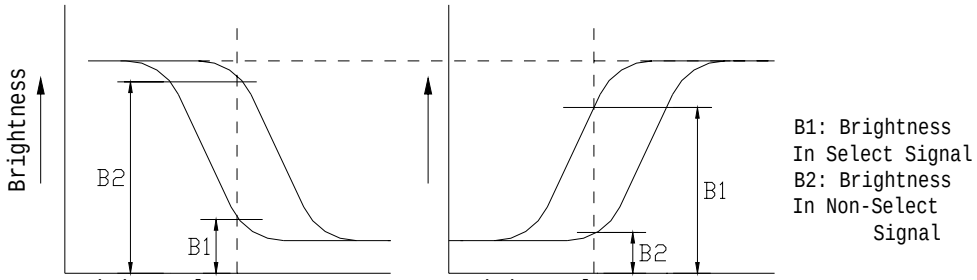
5. MEASUREMENT METHOD OF OPTICAL CHARACTERISTICS

● Definition of Optical Response Time



In case of Negative type,
wave from of changing brightness becomes reverse
(Non Select Signals:0%,Select Signals:100%

● Definition of Contrast Ratio(CR)

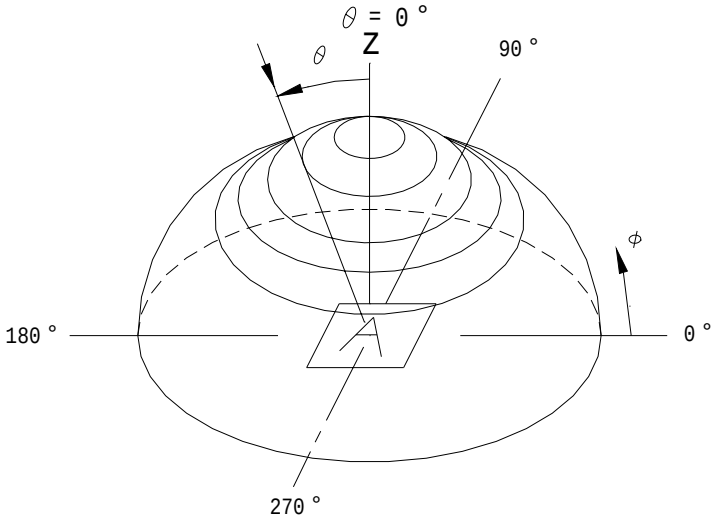


B1: Brightness In Select Signal
B2: Brightness In Non-Select Signal

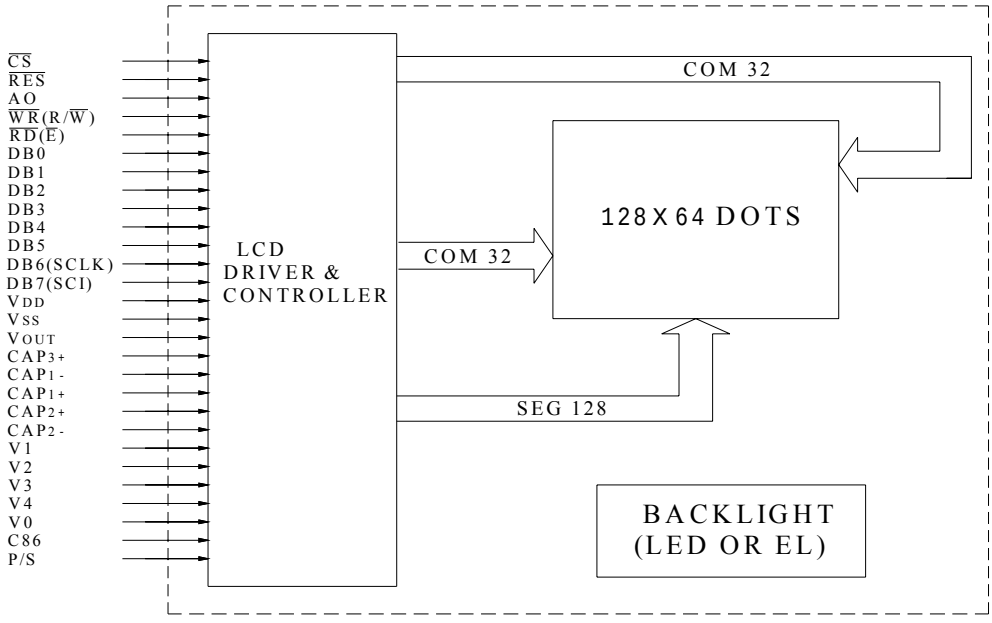
$$CR=\frac{\text{Brightness In Non-Select Signal}}{\text{Brightness In Select Signal}}$$ (Positive Type)

$$CR=\frac{\text{Brightness In Select Signal}}{\text{Brightness In Non-Select Signal}}$$ (Negative Type)

● Definition of Viewing Angle θ and ϕ

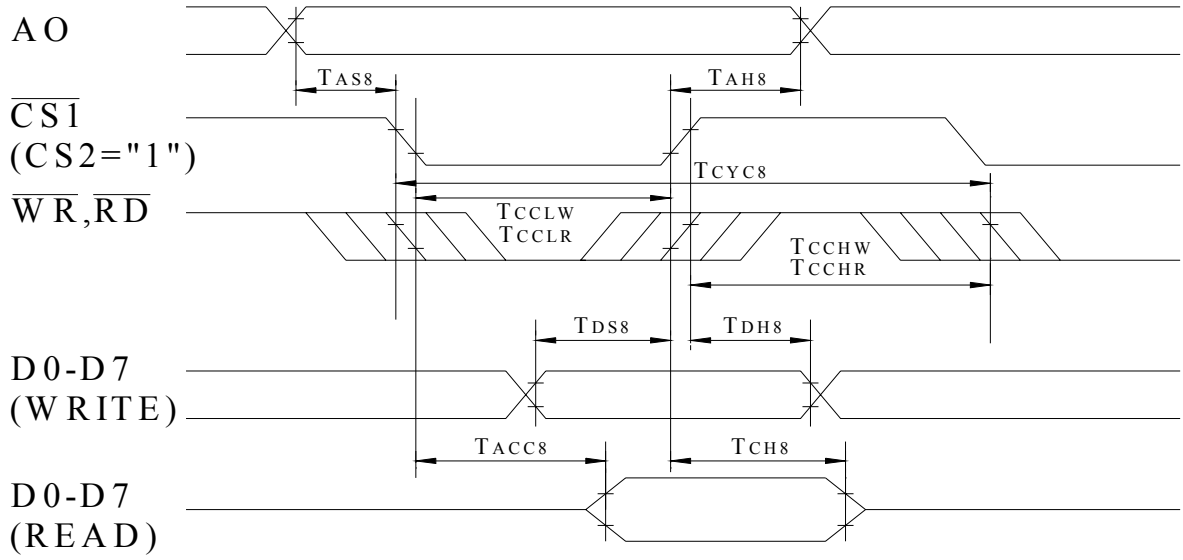


6. BLOCK DIAGRAM



7. SIGNAL TIMING DIAGRAM

7.1. System buses Read/Write characteristics (For the 8080 Series MPU)

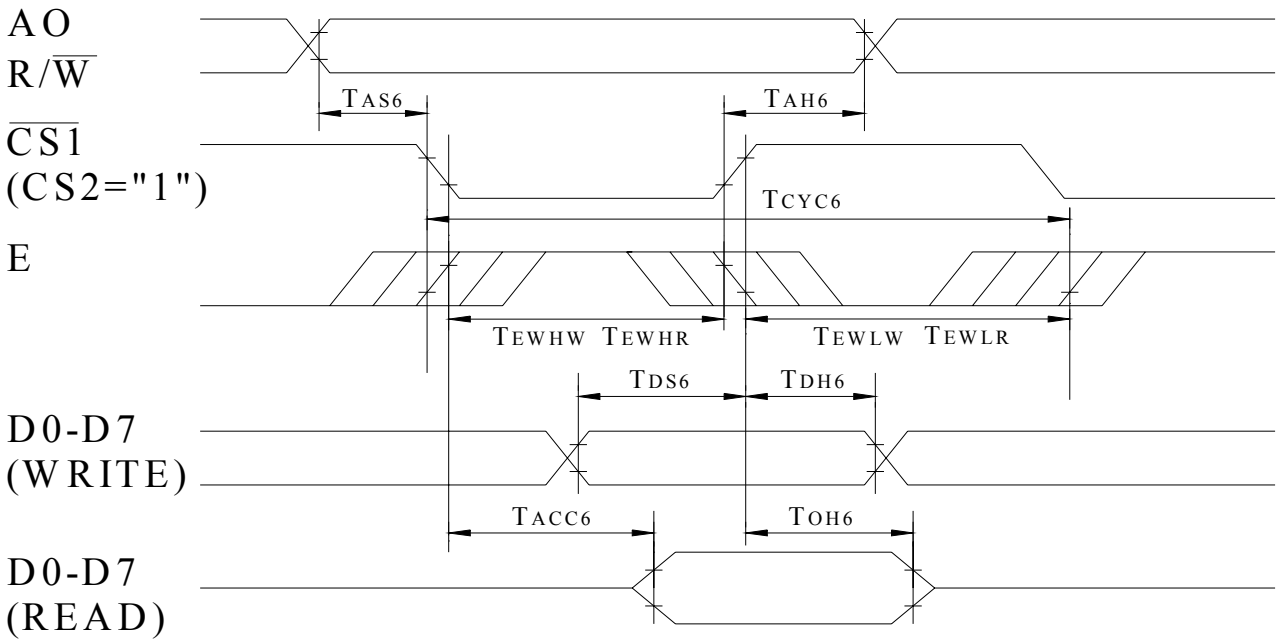


(V_{DD}=2.7~3.3V, T_A=-40~85℃)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Address hold time	T_{AH8}	0	---	---	ns	
Address setup time	T_{AS8}	0	---	---	ns	
System cycle time	T_{CYC8}	300	---	---	ns	
Control L pulse width (WR)	T_{CCLW}	90	---	---	ns	
Control L pulse width (RD)	T_{CCLR}	120	---	---	ns	
Control H pulse width (WR)	T_{CCHW}	120	---	---	ns	
Control H pulse width (RD)	T_{CCHR}	60	---	---	ns	
Data set-up time	T_{DS8}	40	---	---	ns	
Data hold time	T_{DH8}	15	---	---	ns	
/RD access time	T_{ACC8}	---	---	140	ns	C_L=100pF
Output disable time	T_{CH8}	10	---	100	ns	C_L=100pF

1. **The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (T_r+T_f) ≤ (T_{CYC8}-T_{CCLW}-T_{CCHW}) for (T_r+T_f) ≤ (T_{CYC8}-T_{CCLR}-T_{CCHR}) are specified.**
2. **All timing is specified using 20% and 80% of V_{DD} as the reference.**
3. **T_{CCLW} and T_{CCLR} are specified as the overlap between /CS1 being "L" (CS2="H") and /WR and /RD being at the "L" level.**

7.2. System buses Read/Write characteristics (For the 6800 Series MPU)



(V_{DD}=2.7~3.3V, T_A=-40~85℃)

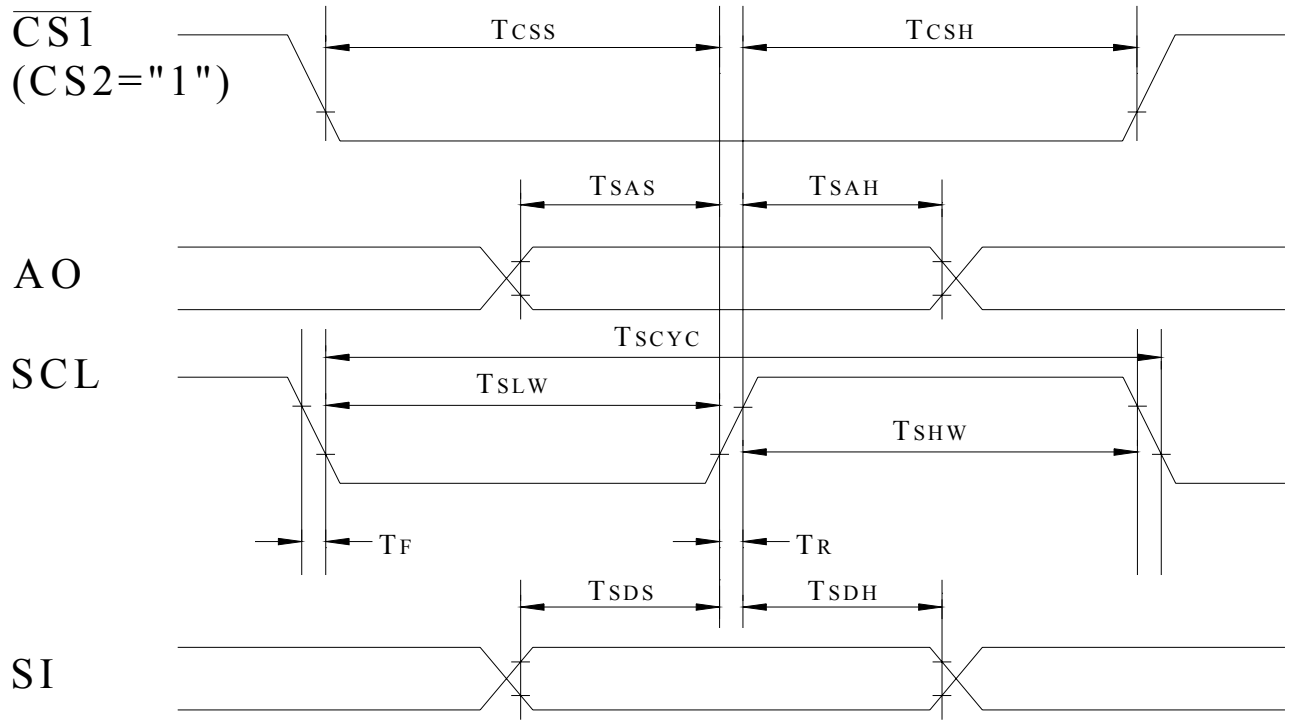
Parameter	Symbol	Min	Typ	Max	Unit	Condition
System cycle time	T_{CYC6}	300	---	---	ns	
Address setup time	T_{AS6}	0	---	---	ns	
Address hold time	T_{AH6}	0	---	---	ns	
Data set-up time	T_{DS6}	40	---	---	ns	
Data hold time	T_{DH6}	15				
Output disable time	T_{OH6}	10	---	100	ns	C_L=100pF
Access time	T_{ACC6}	---	---	140	ns	C_L=100pF
Enable H pulse width (Read)	T_{EWHR}	120	---	---	ns	
Enable H pulse width (Write)	T_{EWHW}	90	---	---	ns	
Enable L pulse width (Read)	T_{EWLR}	60	---	---	ns	
Enable L pulse width (Write)	T_{EWLW}	120	---	---	ns	

1.The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (T_r+T_f) ≤ (T_{CYC6}-T_{EWLW}-T_{EWHW}) for (T_r+T_f) ≤ (T_{CYC6}-T_{EWLR}-T_{EWHR}) are specified.

2.All timing is specified using 20% and 80% of V_{DD} as the reference.

3.T_{CCLW} and T_{CCLR} are specified as the overlap between /CS1 being "L" (CS2="H") and /WR and /RD being at the "L" level.

7.3. Serial interface

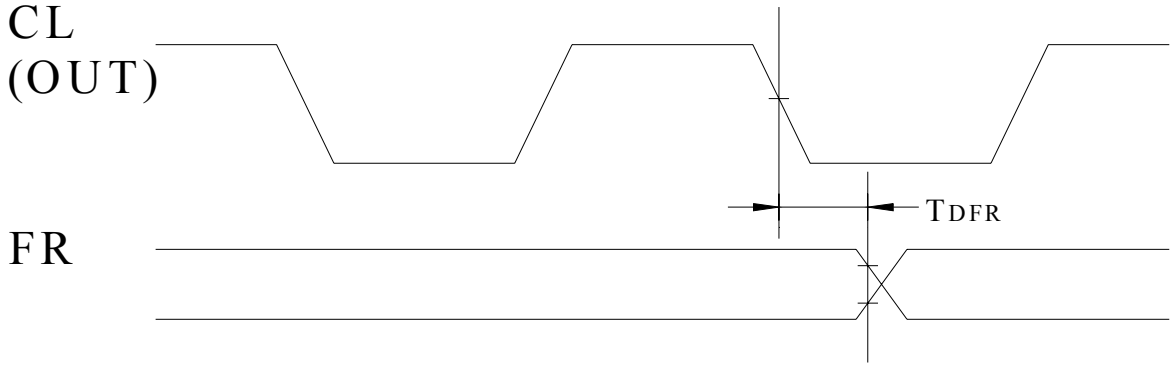


(VDD=2.7~3.3V, TA=-40~85℃)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Serial clock cycle	TSCYC	250	---	---	ns	
Serial clock H pulse width	TSHW	100	---	---	ns	
Serial clock L pulse width	TSLW	100	---	---	ns	
Address setup time	TSAS	150	---	---	ns	
Address hold time	TSAH	150	---	---	ns	
Data set-up time	TSDS	100	---	---	ns	
Data hole time	TSDH	100			ns	
/CS serial clock time	TCSS	150	---	---	ns	
/CS serial clock time	TCSH	150	---	---	ns	

1. **The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less.**
2. **All timing is specified using 20% and 80% of V_{DD} as the standard.**

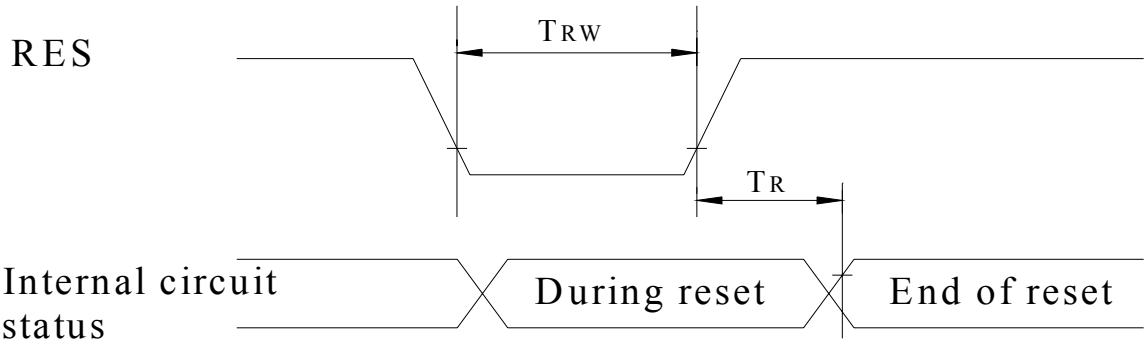
7.4. Display Control Timing



(V_{DD}=2.7~3.3V, T_A=-40~85℃)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FR delay time	T_{DFR}	---	20	80	ns	C_L=50pF

7.5. Reset Timing



(V_{DD}=2.7~3.3V, T_A=-40~85℃)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Reset time	T_R	---	---	1.0	μs	---
Reset L pulse width	T_{RW}	1.0	---	---	μs	---

8 COMMANDS

The NT7532 uses a combination of A0, /RD (E) and /WR(R/W) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.) Accordingly, in the command explanation and command table, /RD (E) becomes 1 (high) when the 6800 series microprocessor interface reads status of display data. This is an only different point form the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example commands will be explained below.

When the serial interface is selected, input data starting from D7 in sequence.

8.1.Command set

8.1-1．Display ON/OFF

Alternatively turns the display on and off.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1 0	Display ON Display OFF

When the display OFF command is executed when in the display all points ON mode, power save mode is entered. See the section on the power saver for details.

8.1-2. Set Display Start Line

Specifies line address (refer to Figure 1) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

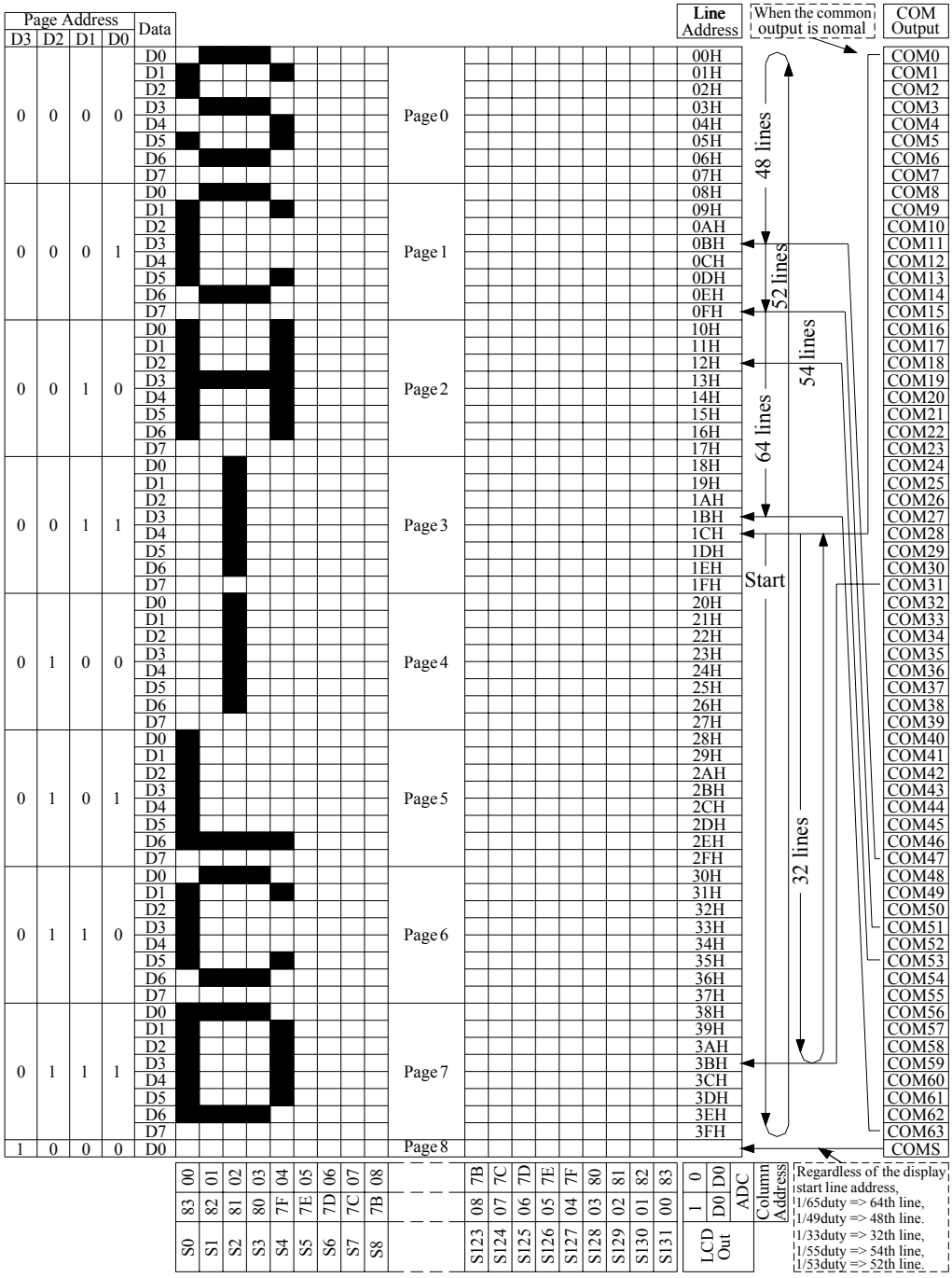


Figure 1

8.1-3. Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Line address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

8.1-4. Set Column Address

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			:					:
1	0	0	0	0	0	1	1	131

8.1-5. Read Status

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7532 is busy due to internal operation or reset. Any command is rejected until BUSY goes low, the busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “132-n” corresponds to segment driver n. When high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is being reset.

8.1-6. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

8.1-7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read

data of multiple words. A single dummy read is-required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8.1-8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremental by 1 as shown in Figure4.

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction).

When D is High, the left rotation (reverse direction).

8.1-9. Normal/Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)

When D is high, the RAM data is low, being LCD ON potential (reverse display)

8.1-10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

8.1-11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Duty 1/33	 1/49	 1/55	 1/65
0	1	0	1	0	1	0	0	0	1	0	1/6 bias	1/8 bias	1/8 bias	1/9 bias
										1	1/5 bias	1/6 bias	1/6 bias	1/7 bias

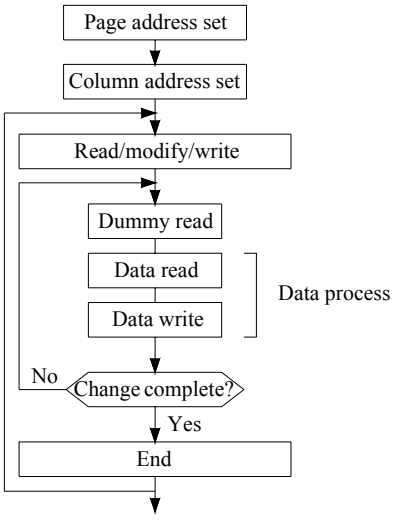
8.1-12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

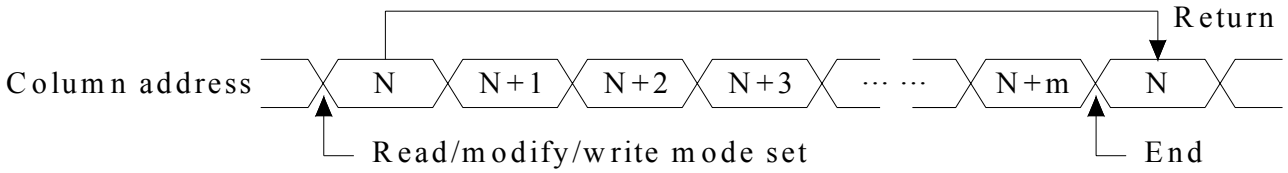
Cursor display sequence



8.1-13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued.)

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



8.1-14. Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

8.1-15. Output Status Select Register

Applicable to the NT7532. When D is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E / $\overline{RD}$	$\overline{R/W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D : Selects the scan direction of COM output pad

D=0: Normal (COM0→COM63/53/47/31) D=1: Reverse (COM63/53/47/31→COM0)

※: Invalid bit

8.1-16. Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.

When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.

When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

8.1-17. Vo Voltage Regulator internal Resistor Ratio Set

This command sets the v0 voltage regulator internal resistor ratio. For details, see the function explanation is “The Power Supply Circuits”.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Rb /Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		
								1	1	0	
								1	1	1	Large

8.1-18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.

This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

■ The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	0	1	
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
0	1	0						:			
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

When the electronic volume function is not used, set the D5- D0 to 100000.

8.1-19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

■ **Static Indicator ON/OFF**

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D=0: Static Indicator OFF D=1: Static Indicator ON

■ **Static Indicator Register Set**

This command sets two bits of data into the static indicator register and is used to set the static indicator into a blinking mode.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON(blinking at approximately 0.5second intervals)
									1	0	ON (blinking at approximately 1 second intervals)
									1	1	ON (constantly on)

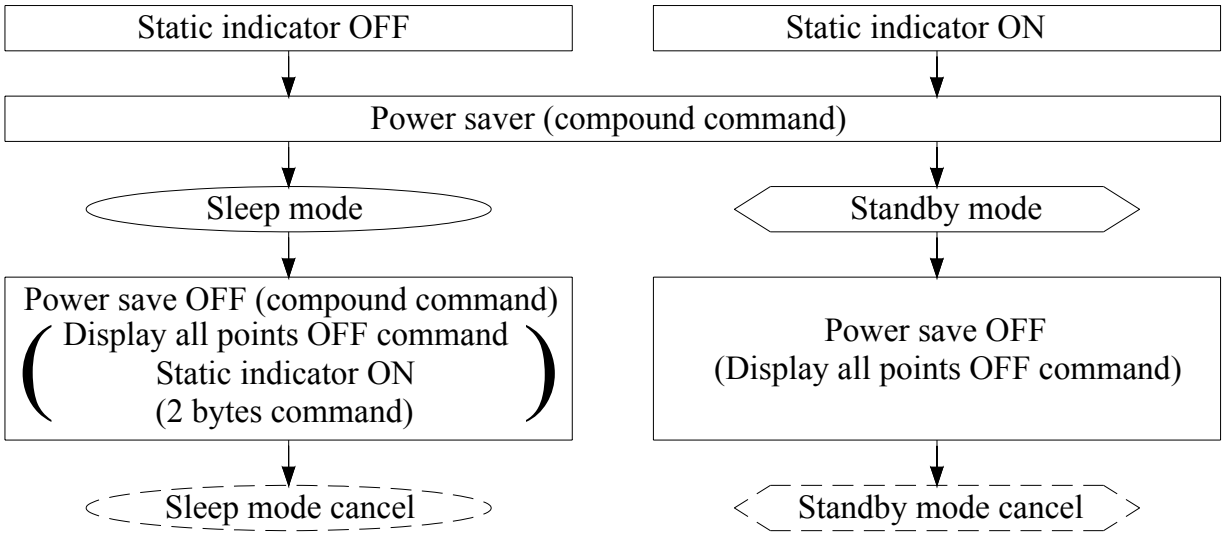
* Disabled bit

8.1-20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce the current consumption.

If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator on command.



Sleep mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is ad follows:

(1) Stops the oscillator circuit and LCD power supply circuit.

(2) Stops the LCD drive and outputs the VSS level as the segment/common driver output

(3) Holds the display data and operation mode provided before the start of sleep mode.

(4) The MPU can access to the built-in display RAM.

Standby mode

Stops the operation of the duty LCD display system and turn on only the static drive system to reduce current consumption to the minimum level required for static drive .

The ON operation of the static drive system indicates that the NT7502 is in the standby mode. The internal status in the standby mode is as follows:

(1) Stop the LCD power supply circuit.

(2) Stop the LCD drive and outputs the VSS level as the segment/common driver output. However, the static drive system operates.

(3) Holds the display data and operation mode provided before the start of the standby mode.

(4) The MPU can access to the built-in display RAM.

When the RESET command is issued in the standby mode , the sleep mode is set.

●When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7532 to go the sleep mode or standby mode.

●When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7502 to go the sleep mode or standby mode.

8.1-21. NOP

Non-operation Command

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

8.1-22. Test Command

This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued unconsciously, set the /RES input to low or issue the Reset command to release the test mode.

A0	E $\overline{RD}$	$\overline{R/W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Invalid bit

Cautions: The NT7532 holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.

The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

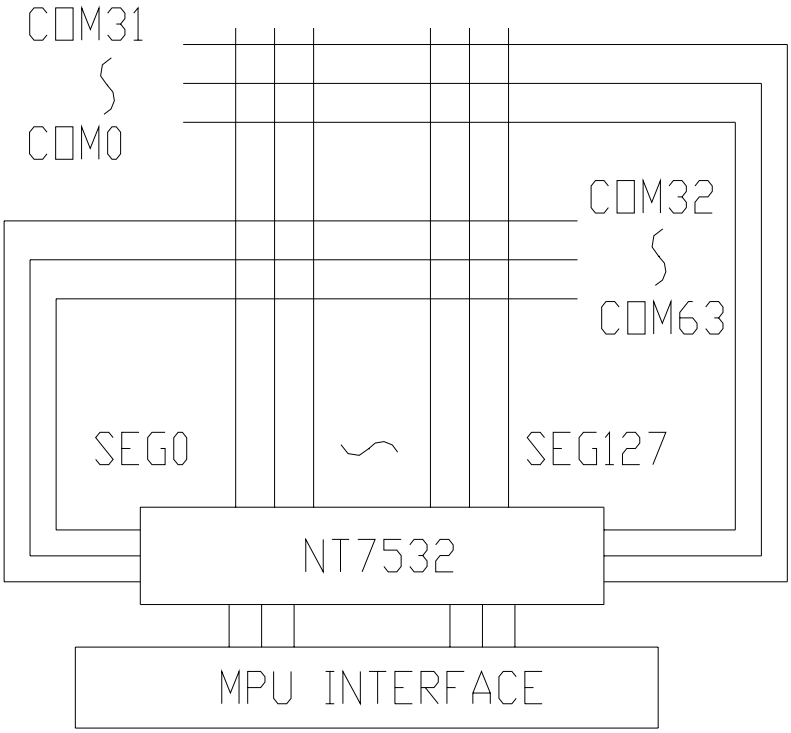
8.2 DISPLAY CONTROL INSTRUCTION

Instruction	A0	RD	WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
1.Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON /OFF, 0: OFF 1: ON
2.Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address.
3.Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address.
4.Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address
5.Status read	0	0	1	Status				0	0	0	0	Reads the status data
6.Display data write	1	1	0	Write data								Writes to the display RAM
7.Display data read	1	0	1	Read data								Reads from the display RAM
8.ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence. 0: normal 1: reverse
9.Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0: normal 1: reverse
10.Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
11. LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD driver voltage bias. 0:1/9 1: 1/7
12.Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment counter during each write
13.End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
14.Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
15.Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction

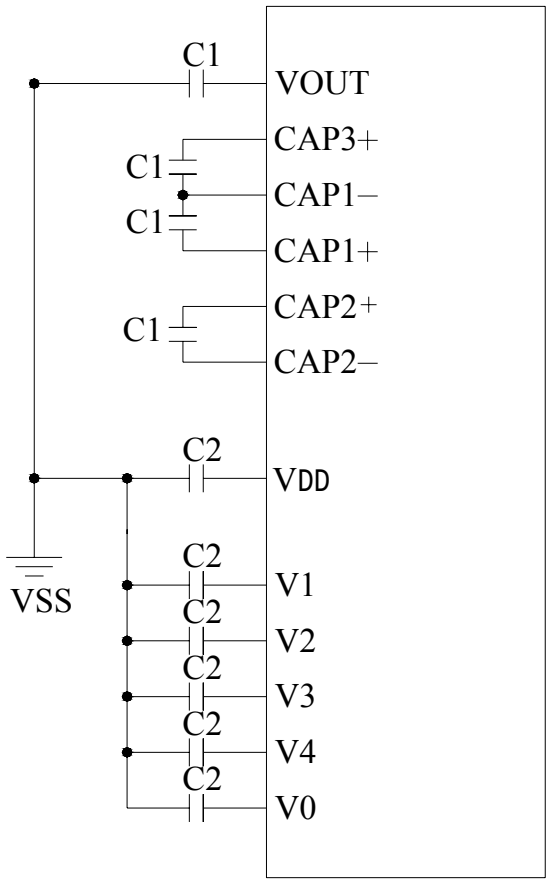
16.Power control set	0	1	0	0	0	1	0	1	Operating mode				Select internal power supply operating mode
17.V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio				Select internal resist or ratio (Rb /Ra) mode
18.Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1		
Electronic volume register set	0	1	0	*	*	Electronic volume value							Set the V0 output voltage electronic volume register
19.Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	1	0: OFF 1: ON
Static indicator register set	0	1	0	*	*	*	*	*	*	Mode			Set the flashing mode
20.Power saver													Display OFF and display all points ON compound command
21.NOP	0	1	0	1	1	1	0	0	0	1	1		Command for non-operation
22.Test Command	0	1	0	1	1	1	1	*	*	*	*		IC Test command. DO not use!
23.Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0		Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

9. DISPLAY DATA RAM ADDRESS MAP



10. THE POWER SUPPLY CRICUITS



C1=C2=1μF

11. RELIABILITY TEST

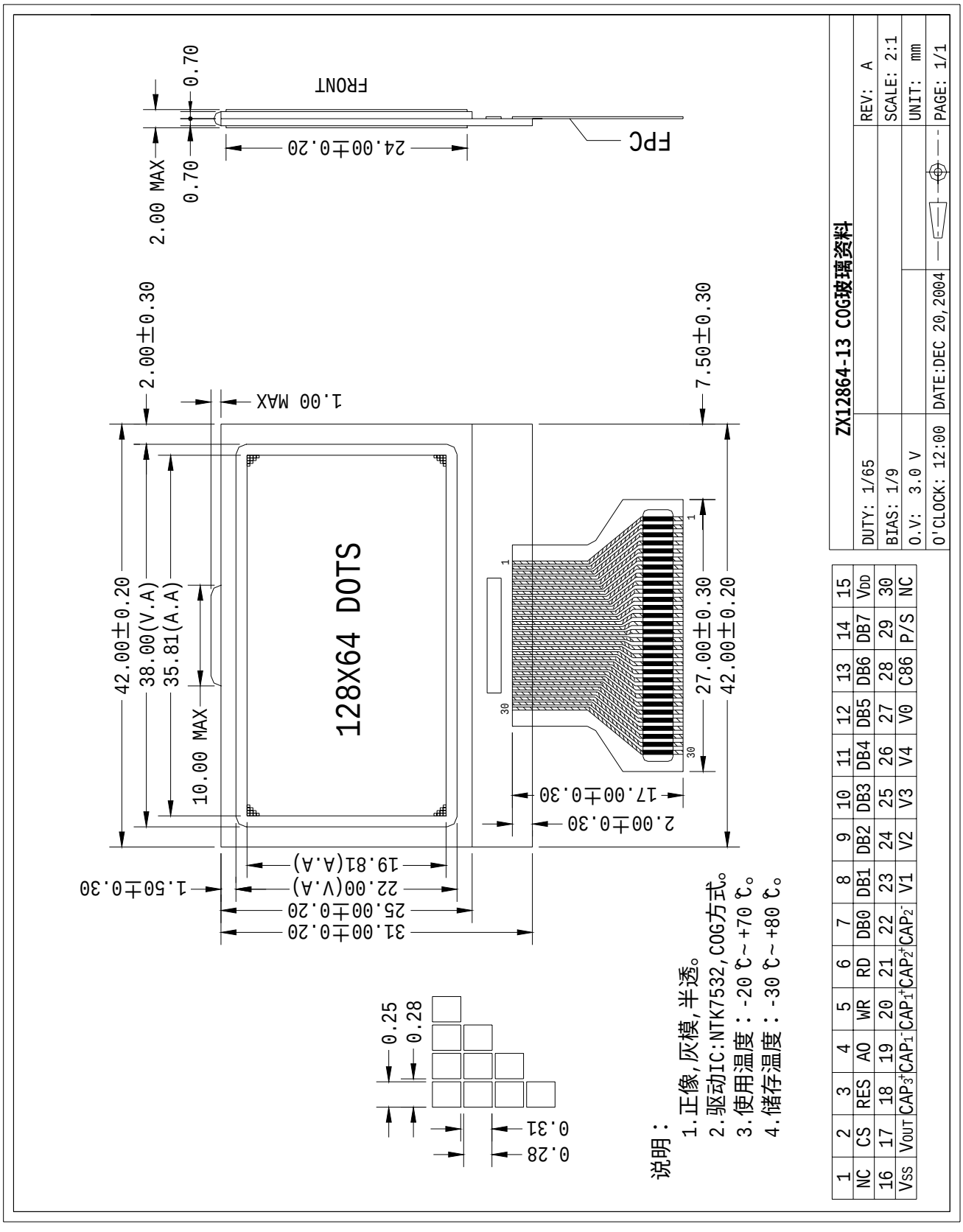
V_{DD}=3V Ta=25℃

Item	Condition	Standard	Note
High temp. storage	80℃,120 hrs	Appearance without defect	---
Low temp. storage	− 30℃,120 hrs	Appearance without defect	---
High temp. operation	70℃,240 hrs	Appearance without defect	---
Low temp. storage	− 20℃,240 hrs	Appearance without defect	---
High temp. & humi. storage	50℃,90% RH,120 hrs	Appearance without defect	---
High temp .& humi. operation	40℃,90% RH,120 hrs	Appearance without defect	---
Thermal shock	-20 ℃ ,30min → +25 ℃ ,5min → +60 ℃,30min	Appearance without defect	10 cycles

12. INTERNAL PIN CONNECTIONS

Pin No.	Symbol	Level	Function
1	NC	---	No connector
2	/CS	L	Chip select signal
3	/RES	L	Reset signal
4	A0	H/L	H: DB0-DB7 are display control data L: DB0-DB7 are display data
5	/WR (R/W)	L	When 8080 MPU /WR→L When 6800 series MPU R/W→H: read R/W→L: write
6	/RD (E)	L	When 8080 MPU /RD→L When 6800 series MPUE→H
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6 (SCL)	H/L	Data bit 6 (SCL) : serial data input
14	DB7 (SI)	H/L	Data bit 7 (SI): serial clock input
15	VDD	3.0V	Supply voltage for logic
16	VSS	0V	Ground
17	VOUT	---	DC/DC voltage converter output
18	CAP3+	---	Capacitor 3+ pad for internal DC/DC voltage converter
19	CAP1-	---	Capacitor 1- pad for internal DC/DC voltage converter
20	CAP1+	---	Capacitor 1+ pad for internal DC/DC voltage converter
21	CAP2+	---	Capacitor 2+ pad for internal DC/DC voltage converter
22	CAP2-	---	Capacitor 2- pad for internal DC/DC voltage converter
23	V1	---	LCD driver supply voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be the following relationship:V1≧V2≧V3≧V4≧V0≧VSS When the on-chip operating power circuit is on, the internal voltages are given to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the set LCD bias command.
24	V2	---	
25	V3	---	
26	V4	---	
27	V0	---	
28	C86	H/L	H : 6800 series MPU interface L : 8080 MPU interface
29	P/S	H/L	H : parallel data input L : serial data input
30	NC	---	No connector

13. DIMENSIONAL OUTLINE



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
NC	CS	RES	AO	WR	RD	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	V_{DD}
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
V_{SS}	V_{OUT}	CAP_3^+	CAP_1^-	CAP_1^+	CAP_2^+	CAP_2^-	V1	V2	V3	V4	V0	C86	P/S	NC

14. PRECATIONS IN USE OF LCD MODULE

14.1 LCD MODULE

▼Precautions for handling LCD modules

Our LCM have been assembled and adjusted accurately before delivery; therefore, observe the following points for handing:

(1) Do not subject it to excessive shocks by dropping it.
(2) Do not modify the tab of the metal holder nor make any arrangement to it.
(3) Do not work on the printed circuit board
(4) Limit the soldering to the printed circuit board only to I/O terminals.
(1)Do not touch the connection rubber (inter-connector), nor modify is location.

▼warning for static electricity

Our LCM uses CMOS LSI. Therefore, cuntermeasures for static electricity is taken through all the process from manufacturing into shipping. When using, taken sufficient care to prevent static electricity as in the case of a normal CMOS IC.

(1) Do not take LCM from its packing bag until it is assembled.
LCM are individually packing in bags treated to resist static electricity. Control them so they are not taken out of the bag until just before the soldering operation for the LCM terminals. When storing them keep them as packed in the bags, or store them in a container processed to be resistant to static electricity, or in a electric conductive container.

(2) Always use a human body grounded when handing LCM.
Always apply grounding to your body while you are working with LCM from the time it is taken out of the anti-static bag until it is assembled in a set to keep the human body and LCM at the same potential. When it is necessary to transfer LCM after it is taken out of the bag, always place it in a electric conductive container.
Moreover, avoid wearing clothes of chemical fiber. Cotton or conductive treated fiber clothes are recommended.

(3) Use a no-leak iron for soldering LCM.
The soldering iron to be used for soldering of I/O terminals LCM, is to be insulated at the iron tip, or grounded at the iron tip.

(4) Grounded electrical apparatus are always required for assembly.
Electrical apparatuse required to assemble LCM in set, specially electric drivers, are to be grounded to avoid the efforts of transmitting spike noise generated when the motor is rotated.

(5) Make the potential of operation bench equal to the grounded potential.
When the operation bench is grounded with aluminum or steel plate, there is a possibility of damag-ing the LCM, or in race cases of electric shocks being generated because the impedance is too low; therefore, it is recommended to use an electric conductive(rubber) mat.

(6) Peel off the LCM protective film slowly.
Our LCM are attached with protective film to protect the display surface from contanmination, flaw, adhesion of flux, etc, however, peeling it off abruptly may cause some static electricity to be generated, so pay attention when peeling off the tape slowly.

(7) Pay attention to the humidity of the work shop.

50~60%RH is statisfactory.

▼Cautions for soldering to LCM

The following shall be soldering the LCM, as already explained:

※ Soldering is to be applied only to the I/O terminals.

※ Use a soldering iron with no leakage.

In addition to the above, pay attention to be following.

(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280℃+10℃

Soldering time: 3-4sec./terminal

Type of solder: Eutectic solder (rosin flux filled)

Avoid using flux, because it may penetrate the LCM , and the LCM may be contaminated when cleaning is required. Moreover, peel off the protective film after soldering the I/O terminals is completed. In this way surface contamination caused by the dispersion of flux while soldering can be avoided.

(2) Removing the wiring

When a lead wire or a connector solder to the I/O terminals of LEM is to be removed, remove it after the solder at the connection part has melted sufficiently because the I/O terminals is insterted into a through hole. If forcefully removed, it may cause the terminal to break or peel. It is recommended to use a suction-type solder sucker. Moreover, do not repeat wiring by soldering more than 3 times.

▼Long-term storage

When long-term storage of MDL is necessary, please com-ply with the following procedure:

If the method of storage is bad, deterioration of the display waterial (polarizer), generation of oxide on the I/O terminals plating (flush plating with gold) may make the soldering process difficult (adhesion of solder becomes worse).

(1) Store as packed in the condition it is delivered from us as far as possible.

(2) If the LCM is independent, place it in anti-static bag, seal the opening, and store it where it is not subjected to direct sunshine, or to the light of a fluorescent lamp.

(3) In either case store them in the temperature rang of 0℃~35℃ and at low humidity.

Please refer to a separated specification sheet for each module about requirement of storage temperature and humidity resistance.

▼Excess electric current protection

Excess electric current protection circuit is not equipped in LCM. Therefore, in preparing for the worst, use electric source which has excess electric current protection circuit.

14.2 PRECAUTIONS IN USE OF LCDS

(1) Do not give any external shock.
(2) Do not wipe the surface with hard materials.
(3) Do not apply excessive force on the surface.
(4) Do not drive by DC voltage.
(5) Do not expose to direct sunlight or fluorecent light for a long time.
(6) Avoid storage in high temperature and high humidity.
(7) When storage for a long time at 40℃ or higher is required, R/H shall be less than 60%.
(8) Liquid in LCD is hazardous substance. Must not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.