中显液晶
技术资料

中显ZX12864E-3使用说明书

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北京市海淀区中关村大街32号和盛大厦811室
电话：(86)-010-52926620　　传真：(86)-010-52926621
企业网站：http://www.zxlcd.com

PRODUCTION CODE: 12864E-3-1FPD-SWE

CONTENTS

1. MECHANICAL DATA

Item	Contents	Unit
LCD Mounting mode	COG, LCD, FPC	
LCD Display mode	Reflective, Transflective and positive	
LCD Display type	STN: Yellow Green mode, Gray mode, Blue mode	
	FSTN	
Viewing direction	6 O'clock or 12 O'clock	
LCD Module size	70.0(W)×50.0(H)×8.0(D,MAX)	mm
LCD Viewing area	54.0(W)×31.0(H)	mm
LCD Display format	128×64 dot matrix	
Dot size	0.34(W)×0.37(H)	mm
Dot pitch	0.38(W)×0.41(H)	mm
LCD Duty	1/65	
LCD Bias	1/9	
LCD Controller/driver LSI	ST7565P (COG)	
LCM Operation temperature (N*)	0~+50	℃
LCM Storage temperature (N*)	-10~+60	℃
LCM Operation temperature (E*)	-20~+70	℃
LCM Storage temperature (E*)	-30~+80	℃
Back light	Edge light LED: Green, White, Blue, Amber	
	EL: White, Yellow green, Blue	
Input data	8080 MPU Interface	
	6800 Series MPU Interface	
	Series data input	
	Parallel data input	
Power supply	2.8-5.5V single power input.	V
	Built- in DC/DC converter for LCD driving.	
	High-accuracy voltage adjustment circuit(thermal gradient –0.05%/℃)	
LCD Expected life	50,000	Hours

NOTICE:

LED*: LED Backlight
EL or None*: EL Backlight or no backlight
N*: Normal temperature type
E*: Extended temperature type

2. ABSOLUTE MAXIMUM RATINGS

2.1 ELECTRICAL ABSOLUTE RATINGS

V_{SS} =0V

Item	Symbol	Min	Max	Unit	Note
Power supply for logic	V_{DD}-V_{SS}	-0.3	7.0	V	
Power supply for LCD	V_{DD}-Vo	-0.3	12.0	V	
Input voltage	Vi	-0.3	Vdd+0.3	V	

2.2 ENVIRONMENTAL ABSOLUTE RATINGS

Item		Symbol	Min	Max	Unit
Normal type	Operating temperature	T0	0	+50	℃
	Storage temperature	Ts	-10	+60	℃
Wide type	Operating temperature	T0	-20	+70	℃
	Storage temperature	Ts	-30	+80	℃
Humidity		---	---	85	%RH

3. ELECTRRICAL CHARACTERISTICS

3.1 ELECTRRICAL CHARACTERISTICS

V_{SS}=0V

Item		Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	Logic	V_{DD}	----	2.8	3.0	5.5	V
	Booster output	V_{OUT}	----	6.0		12.0	V
	LCD drive	Vo	----	4.5	---	11.5	V
High-level input voltage		V_{IHC}	----	0.8V_{DD}	---	V_{DD}	V
Low- level input voltage		V_{ILC}	----	V_{SS}	---	0.2V_{DD}	V
High-level output voltage		V_{OHC}	I_{OH}=-0.5mA	0.8V_{DD}	---	V_{DD}	V
Low- level output voltage		V_{OLC}	I_{OL}=0.5mA	V_{SS}	---	0.2V_{DD}	V
Sleep mode		I_{SP}	25℃	---	0.01	5.0	μA
Standby mode		I_{SB}	25℃	---	4.0	8.0	μA

3.2 SPECIFICATION FOR LED BACKLIGHT

■ EDGE LIGHT BACKLIGHT

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	4.0	4.2	4.4	
LED Consumption current	mA	-	45	-	
LED Color		Yellow Green			

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	2.8	3.2	3.6	
LED Consumption current	mA	-	60	-	
LED Color		White			

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	2.8	3.2	3.6	
LED Consumption current	mA	-	60	-	
LED Color		Blue			

Item	Unit	Min	Typ	Max	Condition
LED Supply voltage	V	1.7	1.9	2.1	
LED Consumption current	mA	-	30	-	
LED Color		Amber			

3.3 SPECIFICATION FOR EL BACKLIGHT

Item	Unit	Min	Typ	Max	Condition
Supply voltage	V	---	100	125	
Supply frequeney	Hz	---	400	400	
Initial brightness	cd/m	40	---	--	AC 100Vrms,400Hz,Dark room
Current	mA	3.3_+30%			AC 100Vrms,400Hz,Dark room
Operating temperature	℃	-20~+50			
Storage temperature	℃	-20~+60			
Luminous color	--	White			AC 100Vrms,400Hz,Dark room
Life time	Hrs	3,000			Note 1

Note 1: Half value of initial brightness at 20℃ 60%RH

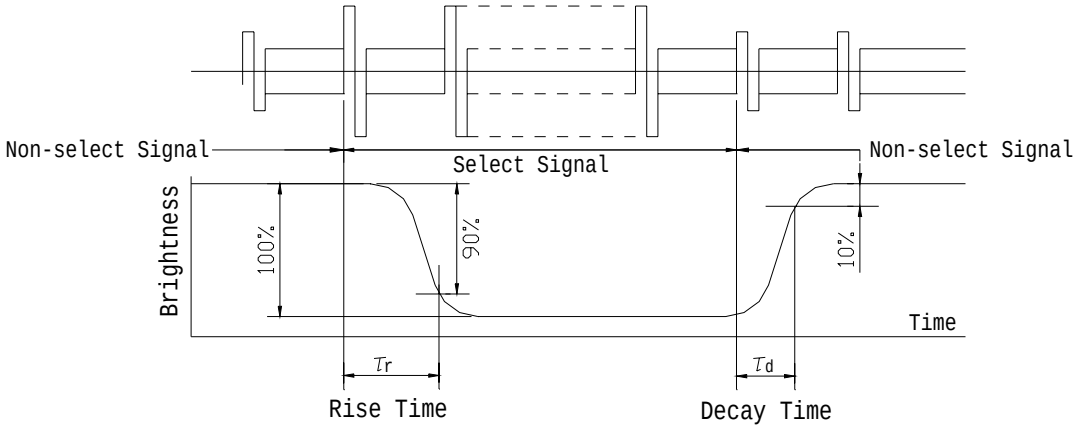
4. OPTICAL CHARACTERISTICS

STN TYPE Ta=25℃

Item	Symbol	Condition	Min	Typ	Max	Unit	Reference
Viewing angle	θ	K≧2.0 ϕ=0o	40o	---	---	deg	Note1,2
Contrast ration	K	θ=5o ϕ=0o	---	5	---	---	Note3
Response time (rise)	Tr	θ=5o ϕ=0o	---	110	165	ms	Note4
Response time (fall)	Tf	θ=5o ϕ=0o	---	110	165	ms	Note4

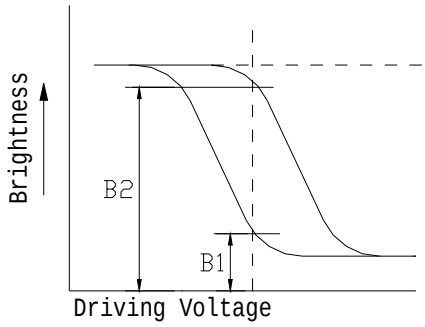
5. MEASUREMENT METHOD OF OPTICAL CHARACTERISTICS

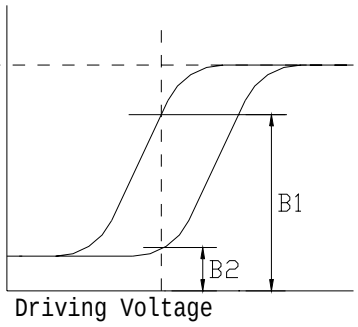
● Definition of Optical Response Time



In case of Negative type,
wave from of changing brightness becomes reverse
(Non Select Signals:0%,Select Signals:100%

● Definition of Contrast Ratio(CR)



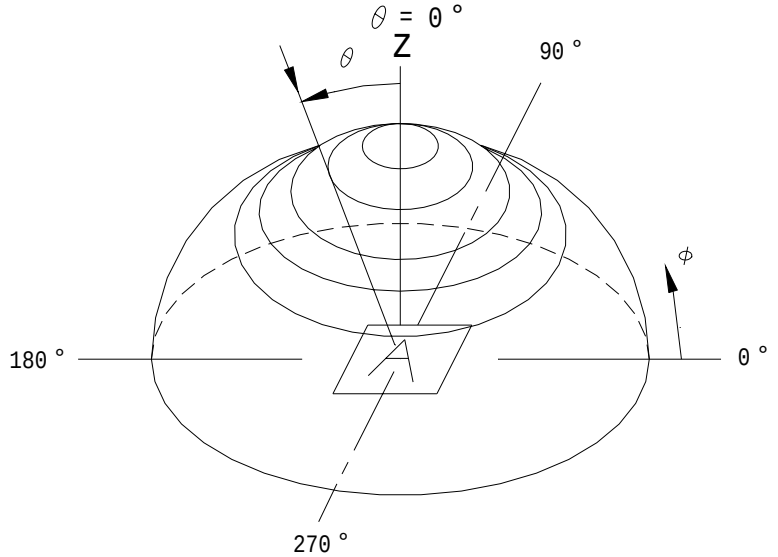


B1: Brightness
In Select Signal
B2: Brightness
In Non-Select
Signal

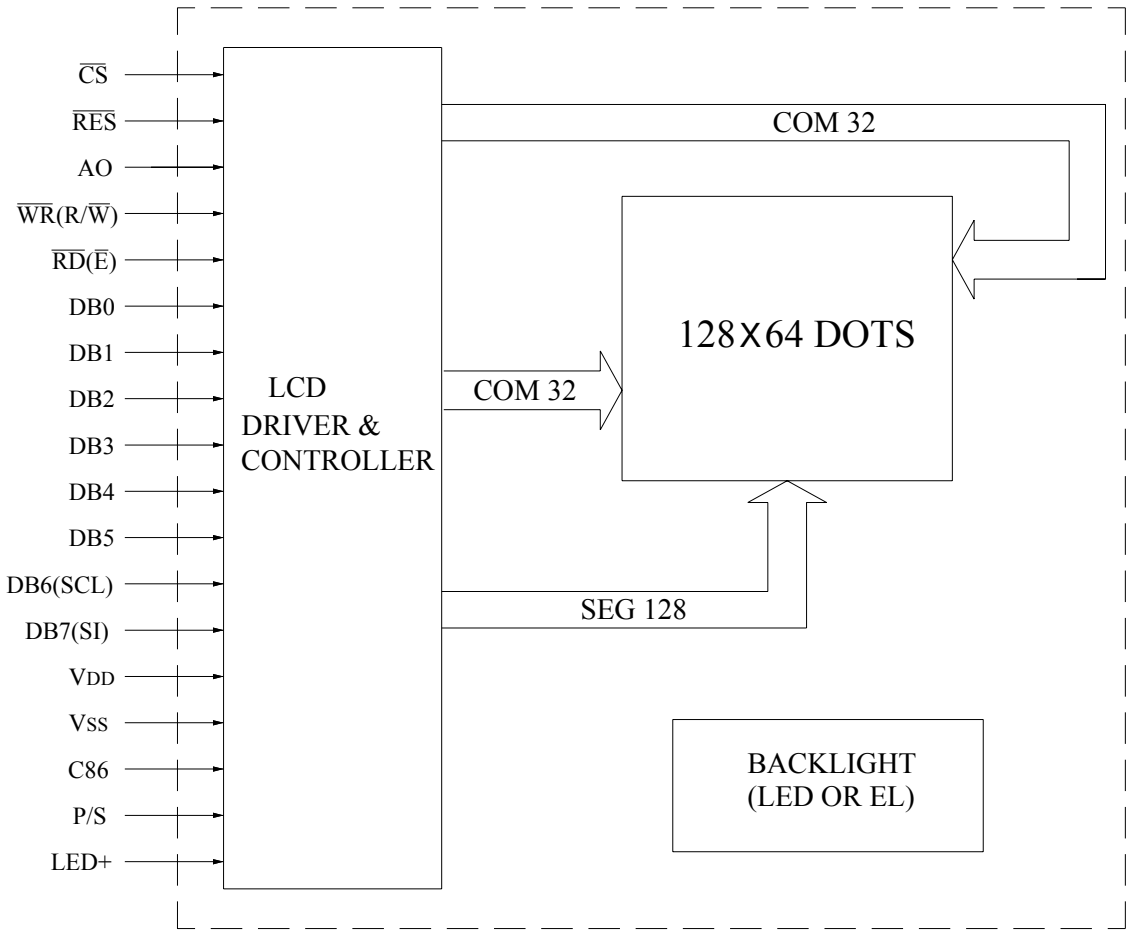
$$CR=\frac{\text{Brightness In Non-Select Signal}}{\text{Brightness In Select Signal}}$$
(Positive Type)

$$CR=\frac{\text{Brightness In Select Signal}}{\text{Brightness In Non-Select Signal}}$$
(Negative Type)

● Definition of Viewing Angle θ and ϕ

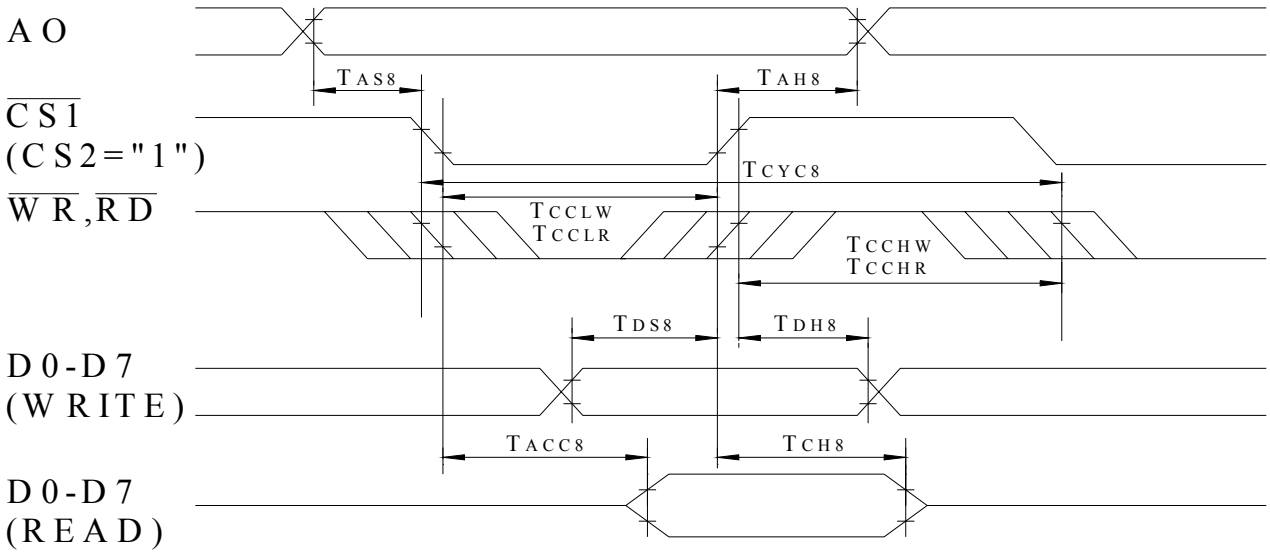


6. BLOCK DIAGRAM



7. SIGNAL TIMING DIAGRAM

7.1. System buses Read/Write characteristics (For the 8080 Series MPU)



(V_{DD}=3.3V, T_A=25℃)

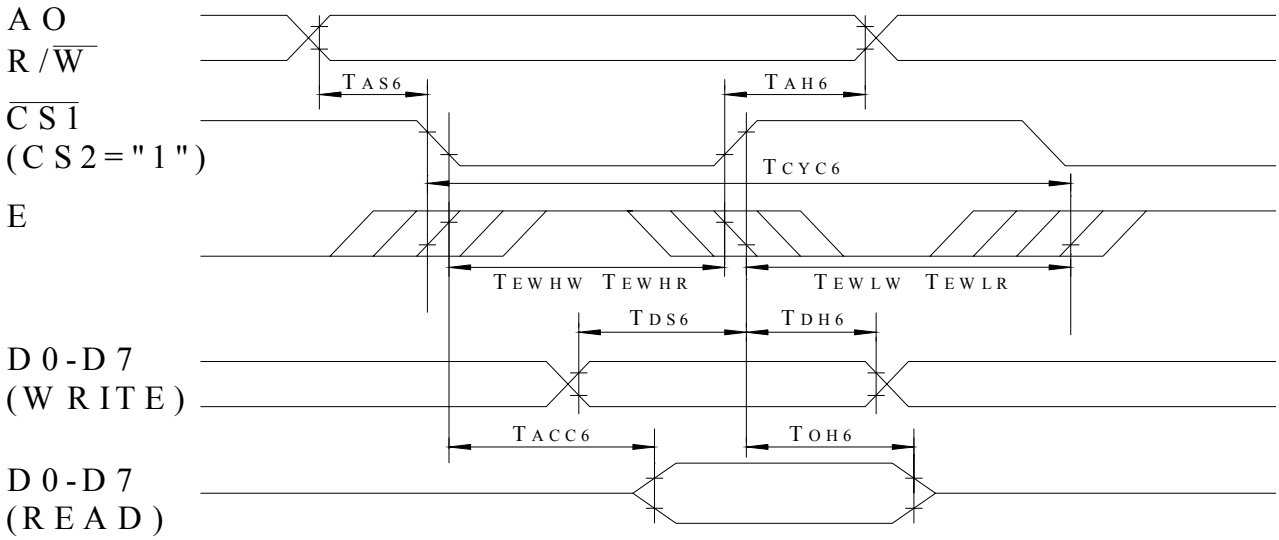
Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Address hold time	A0	T_{AH8}	0	---	---	ns	
Address setup time		T_{AS8}	0	---	---	ns	
System cycle time		T_{CYC8}	240	---	---	ns	
Control L pulse width (WR)	WR	T_{CCLW}	80	---	---	ns	
Control L pulse width (RD)	RD	T_{CCLR}	140	---	---	ns	
Control H pulse width (WR)	WR	T_{CCHW}	80	---	---	ns	
Control H pulse width (RD)	RD	T_{CCHR}	80	---	---	ns	
WRITE Data set-up time	D0 | D7	T_{DS8}	40	---	---	ns	
WRITE Data hold time		T_{DH8}	0	---	---	ns	
READ access time		T_{ACC8}	---	---	70	ns	C_L=100pF
READ Output disable time		T_{CH8}	5.0	---	50	ns	C_L=100pF

(V_{DD}=2.7V, T_A=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Address hold time	A0	T_{AH8}	0	---	---	ns	
Address setup time		T_{AS8}	0	---	---	ns	
System cycle time		T_{CYC8}	400	---	---	ns	
Control L pulse width (WR)	WR	T_{CCLW}	220	---	---	ns	
Control L pulse width (RD)	RD	T_{CCLR}	220	---	---	ns	
Control H pulse width (WR)	WR	T_{CCHW}	180	---	---	ns	
Control H pulse width (RD)	RD	T_{CCHR}	180	---	---	ns	
WRITE Data set-up time	D0 | D7	T_{DS8}	40	---	---	ns	
WRITE Data hold time		T_{DH8}	0	---	---	ns	
READ access time		T_{ACC8}	---	---	140	ns	C_L=100pF
READ Output disable time		T_{CH8}	10	---	100	ns	C_L=100pF

1. **The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (T_r+T_f) ≤ (T_{CYC8}-T_{CCLW}-T_{CCHW}) for (T_r+T_f) ≤ (T_{CYC8}-T_{CCLR}-T_{CCHR}) are specified.**
2. **All timing is specified using 20% and 80% of V_{DD} as the reference.**
3. **T_{CCLW} and T_{CCLR} are specified as the overlap between /CS1 being "L" (CS2="H") and /WR and /RD being at the "L" level.**

7.2. System buses Read/Write characteristics (For the 6800 Series MPU)



(VDD=3.3V, TA=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
System cycle time	A0	TCYC6	240	---	---	ns	
Address setup time		TAS6	0	---	---	ns	
Address hold time		TAH6	0	---	---	ns	
WRITE Data set-up time	D0 | D7	TDS6	40	---	---	ns	
WRITE Data hold time		TDH6	0	---	---	ns	
READ Output disable time		TOH6	5	---	50	ns	CL=100pF
READ Access time		TACC6	---	---	70	ns	CL=100pF
Enable H pulse width (Read)	RD	TEWHR	140	---	---	ns	
Enable H pulse width (Write)	WR	TEWHW	80	---	---	ns	
Enable L pulse width (Read)	RD	TEWLR	80	---	---	ns	
Enable L pulse width (Write)	WR	TEWLW	80	---	---	ns	

(VDD=2.7V, TA=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
System cycle time	A0	TCYC6	400	---	---	ns	
Address setup time		TAS6	0	---	---	ns	
Address hold time		TAH6	0	---	---	ns	
WRITE Data set-up time	D0 | D7	TDS6	40	---	---	ns	
WRITE Data hold time		TDH6	0				
READ Output disable time		TOH6	10	---	100	ns	CL=100pF
READ Access time		TACC6	---	---	140	ns	CL=100pF
Enable H pulse width (Read)	RD	TEWHR	180	---	---	ns	
Enable H pulse width (Write)	WR	TEWHW	180	---	---	ns	
Enable L pulse width (Read)	RD	TEWLR	220	---	---	ns	
Enable L pulse width (Write)	WR	TEWLW	220	---	---	ns	

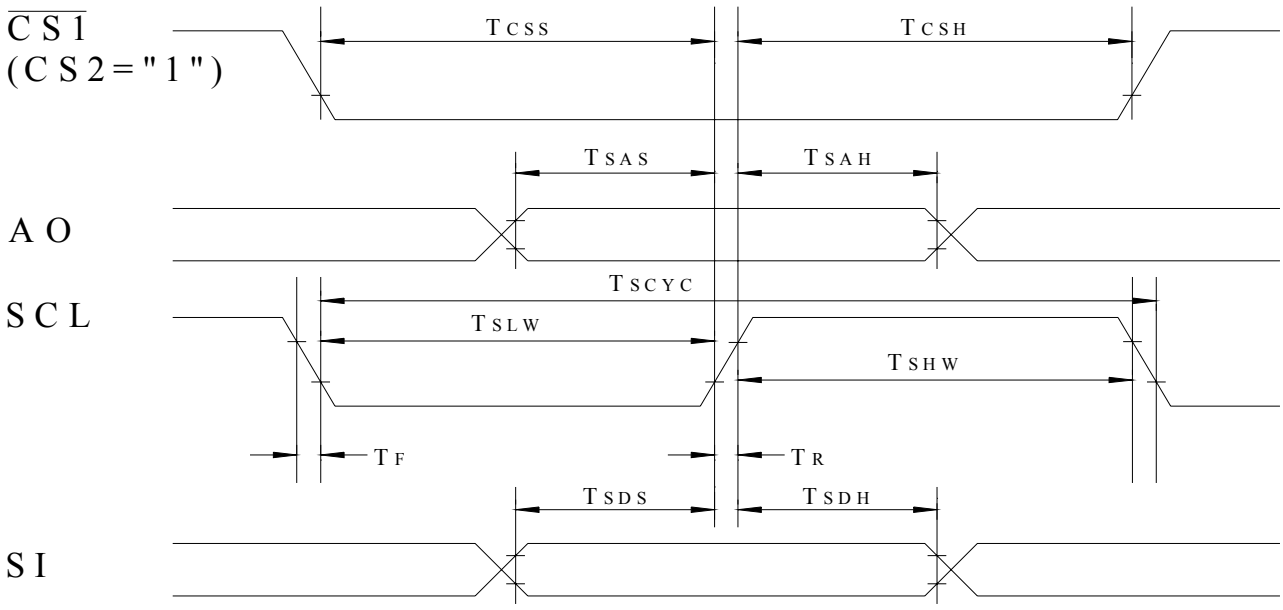
1.The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less. When the system cycle

time is extremely fast, (Tr+Tf) ≤ (TCYC6-TEWLW-TEWHW) for (Tr+Tf) ≤ (TCYC6-TEWLR-TEWHR) are specified.

2.All timing is specified using 20% and 80% of VDD as the reference.

3.TEWLW and TEWLR are specified as the overlap between /CS1 being "L" (CS2="H") and E.

7.3. Serial interface



(VDD=3.3V, TA=25℃)

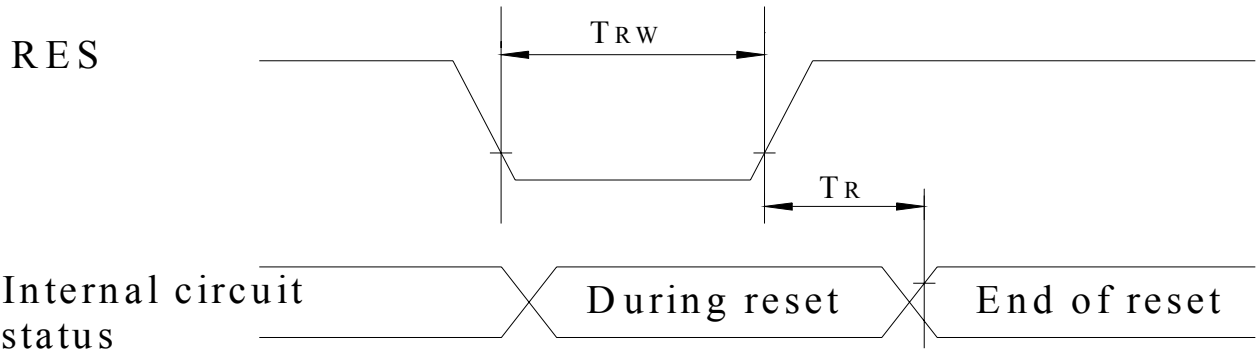
Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Serial clock cycle	SCL	TSCYC	50	---	---	ns	
Serial clock H pulse width		TSHW	25	---	---	ns	
Serial clock L pulse width		TSLW	25	---	---	ns	
Address setup time	A0	TSAS	20	---	---	ns	
Address hold time		TSAH	10	---	---	ns	
Data set-up time	SI	TSDS	20	---	---	ns	
Data hole time		TSDH	10			ns	
/CS serial clock time	CS	TCSS	20	---	---	ns	
/CS serial clock time		TCSH	40	---	---	ns	

(VDD=2.7V, TA=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Serial clock cycle	SCL	TSCYC	100	---	---	ns	
Serial clock H pulse width		TSHW	50	---	---	ns	
Serial clock L pulse width		TSLW	50	---	---	ns	
Address setup time	A0	TSAS	30	---	---	ns	
Address hold time		TSAH	20	---	---	ns	
Data set-up time	SI	TSDS	30	---	---	ns	
Data hole time		TSDH	20			ns	
/CS serial clock time	CS	TCSS	30	---	---	ns	
/CS serial clock time		TCSH	60	---	---	ns	

1. **The input signal rise time and fall time (T_r, T_f) is specified at 15 ns or less.**
2. **All timing is specified using 20% and 80% of V_{DD} as the reference.**

7.4. Reset Timing



(V_{DD}=3.3V, T_A=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Reset time		TR	---	---	1.0	μs	---
Reset L pulse width	/RES	TRW	1.0	---	---	μs	---

(V_{DD}=2.7V, T_A=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Reset time		TR	---	---	2.0	μs	---
Reset L pulse width	/RES	TRW	2.0	---	---	μs	---

(V_{DD}=1.8V, T_A=25℃)

Parameter	Signal	Symbol	Min	Typ	Max	Unit	Condition
Reset time		TR	---	---	3.0	μs	---
Reset L pulse width	/RES	TRW	3.0	---	---	μs	---

Note: All timing is specified with 20% and 80% of VDD as the standard.

8. UNIT DRIVING METHOD

8.1. Explanation of commands

8.1-1.Display ON/OFF

This command turns the display ON and OFF.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed and when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

8.1-2. Display Start line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 1. For further details, see the explanation of this function in 'The Line Address Circuit'.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line Address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
					↓	↓	↓	↓	↓	↓	↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

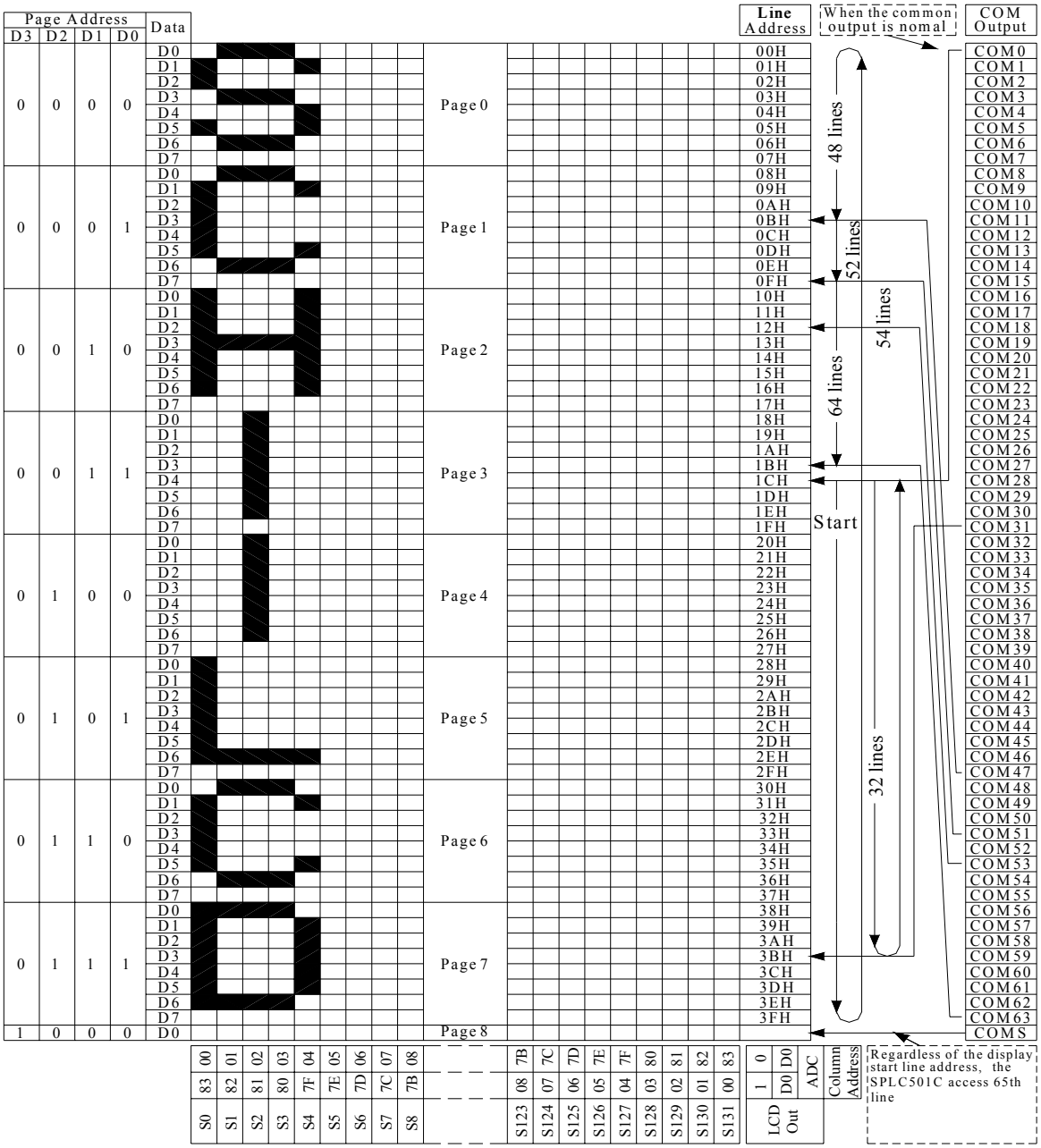


Figure 1

8.1-3. Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 1). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the page address circuit in the function description for the detail.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓	↓	↓	↓	↓
							0	1	1	1	7
							1	0	0	0	8

8.1-4. Column Address Set

This command specifies the column address of the display data RAM shown in Figure 1. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically incremented (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in 'The Column Address Circuit' for details.

	AO	E /RD	RW /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column Address
High bits	0	1	0	1	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	0	0	130
												1	0	0	0	0	0	1	1	131

8.1-5. Status Read

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	/RESET	0	0	0	0

BUSY	When BUSY='1', it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY='0',if the cycle time can be satisfied, there is no need to check for BUSY condition.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ---SEG n) 1: Normal (column address n---SEG n) (The ADC command switches the polarity)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1:Display OFF (This display ON/OFF command switches the polarity)
/RESET	This indicates that the chip is in the process of initialization either because of a /RESET signal or because of a reset command. 0: Operating state. 1: Reset in progress

8.1-6. Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by one after the write, the MPU can write the display data.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

8.1-7. Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by one after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address being set. See the function explanation in 'Display Data RAM' for the explanation of accessing the internal registers. When the serial interface is used, reading the display data becomes unavailable.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8.1-8. ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by '1') according to the column address indicated in Figure 4.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

8.1-9. Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done, the display data RAM contents are maintained.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data 'H'
											LCD ON voltage (normal)
										1	RAM Data 'L'
											LCD ON voltage (reverse)

8.1-10. Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For more details, see the Power save section.

8.1-11. LCD Bias Set

This command selects the voltage bias ratio for the LCD.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Select Status
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

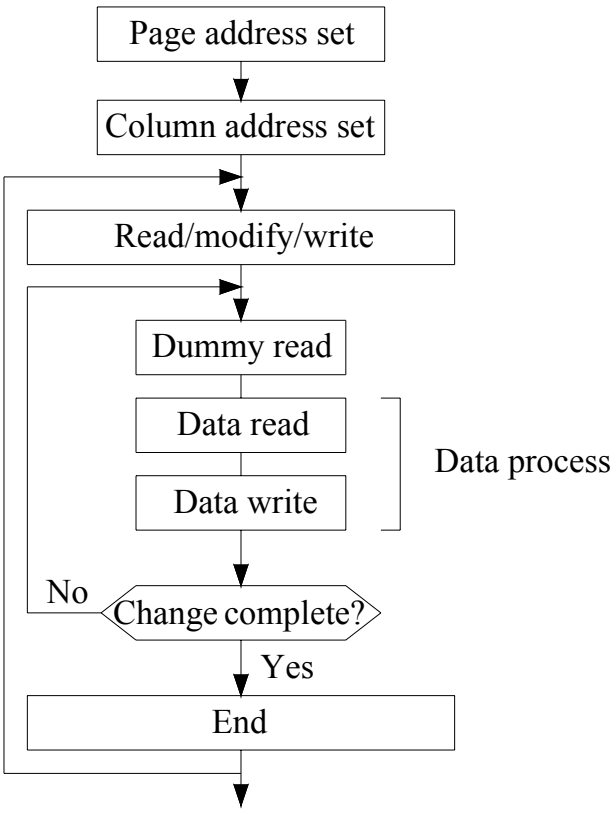
8.1-12. Read/Modify/Write

This command is used paired with the 'END' command. Once this command has been inputted, the display data read command does not change the column address, but only the display data write command increment (+1) the column address. This mode remains until the END command is inputted. When the END command is inputted, the column address returns to the address at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there is repeating data changes in a specified display region, such as when there is a blanking cursor.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Even in read/modify/write mode, other commands aside from display data read/modify/write commands can also be used. However, the column address set command cannot be used.

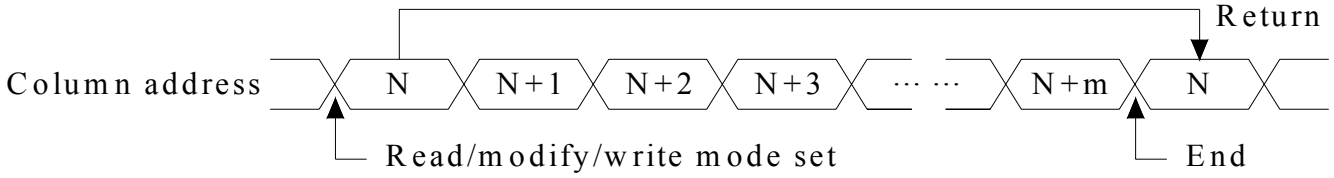
8.1-12.1 The Sequence For Cursor Display



8.1-13. END

This command releases the read/modify/write mode, and returns the column address to the address at when the mode was entered.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



8.1-14. RESET

This command initializes the display start line, the column address, the page address, the common output mode, the V5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in 'RESET' for details. The reset operation is performed after the reset command is entered.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization must be done through applying a reset signal /RESET terminal when the power supply is applied.

8.1-15. Common Output Mode Select

The command can select the scan direction of the COM output terminal. For details, see the function explanation in 'Common Output Mode Select Circuit'.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Select Status
0	1	0	1	1	0	0	0	*	*	*	Normal COM0→COM63
							1				Reverse COM63→COM0

Note: * Disabled bit.

8.1-16. Power Controller Set

This command sets the power supply circuit functions. See the function explanation in 'The Power Supply Circuit ' for more details.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

Note: Display off command masks the power control circuits.

8.1-17. V_0 Voltage Regulator Internal Resistor Ration Set

This command sets the V5 voltage regulator internal resistor ratio. For details, see the function explanation in 'The Power Supply Circuit '.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

8.1-18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the LCD by controlling the liquid crystal drive voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal supply. This command is a two bytes command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

8.1-18.1 The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, the electronic volume mode is released.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

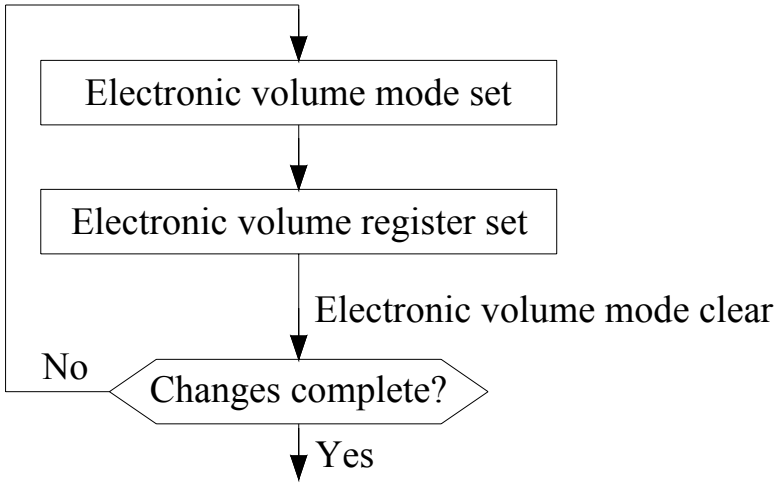
8.1-18.2 Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal driving voltage, V0, assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
						↓					↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

Note: * Inactive bit. When the electronic volume function is not used, set this to (1,0,0,0,0,0)

8.1-18.3 The Electronic Volume Register Set Sequence



8.1-19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent from other display control commands. This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes. The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. The static indicator OFF command is a single byte command.

8.1-19.1 Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command is entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

8.1-19.2 Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting Indicator
0	1	0	*	*	*	*	*	*	0	0	OFF
			*	*	*	*	*	*	0	1	ON (blinking at approximately 0.5 second intervals)
			*	*	*	*	*	*	1	0	ON (blinking at approximately one second intervals)
			*	*	*	*	*	*	1	1	ON (constantly on)

Note: * Disabled bit (set'0').

8.1-20. The Booster Ratio (Double Byte Command)

This command makes it possible to possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte commands used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

8.1-20.1 Booster Ratio Select Mode Set

When this command is input, the booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ration register set command has been used to set data into the register, when the booster ratio select mode is released.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

8.1-20.2 Booster Ratio Register Set

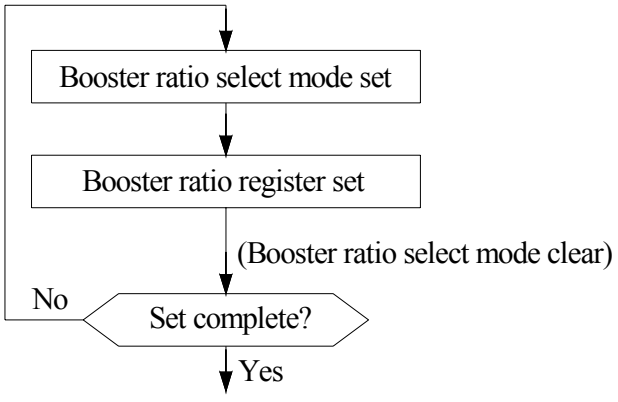
By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used. When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0	Blinking Page
0	1	0	*	*	*	*	*	*	0	0	2×,3× 4×
			*	*	*	*	*	*	0	1	5×
			*	*	*	*	*	*	1	1	6×

Note: * Disabled bit (set'0').

When the booster ratio select function is not used, set this to (0,0) 2×,3×,4× step-up mode.

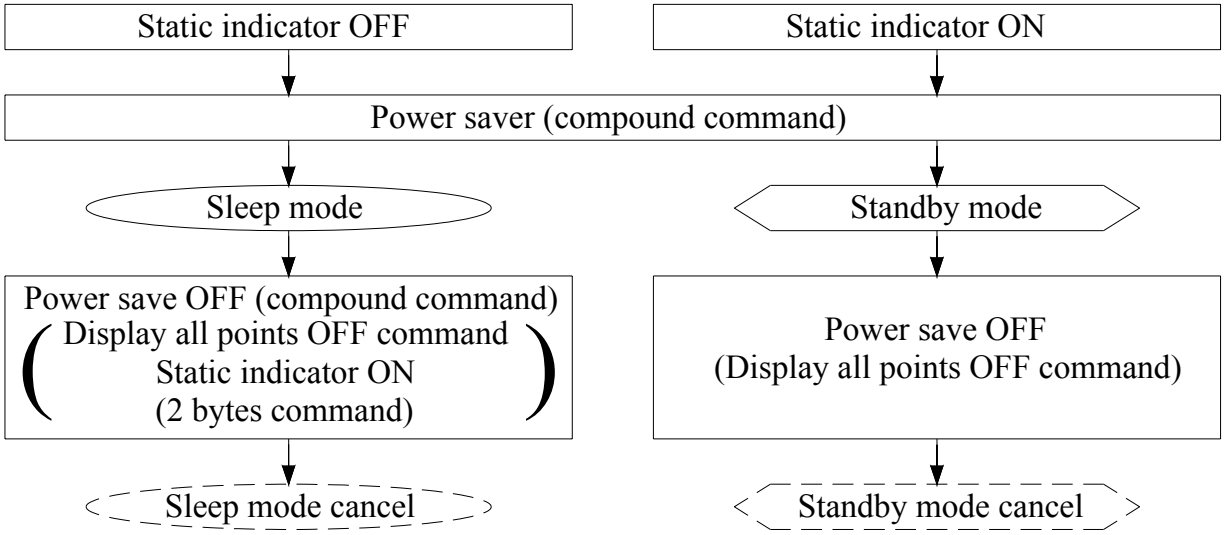
8.1-20.3 The Booster Ratio Register Set Sequence



8.1-21. Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered and therefore, it reduces a great amount of power. The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, the sleep mode is entered.

When the static indicator is ON, the standby mode is entered. In the sleep mode and standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.



8.1-21.1 Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value close to the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VDD level.

8.1-21.2 Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

1. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2. The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs a VDD level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

Note1: When an external power supply is used, it is recommended that the functions of the external power supply circuit should be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The SPLC501C chips have a LCD blanking control terminal /DOF. This terminal enters a ‘L ’ state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.

Note2: When the master is turned on , the oscillator circuit is operable immediately after the power on.

8.1-22 NOP

Non –Operation Command

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

8.1-23. TEST

This is a command for IC chip testing. Please do not use it, if the test command is used by accident, it can be cleared by applying a 'L ' signal to the 'RESET' input by the reset command or by using a NOP.

AO	E (/RD)	RW (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

Inactive bit.

Note: The ST7565P maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc, can change the internal modes of the ST7565P. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

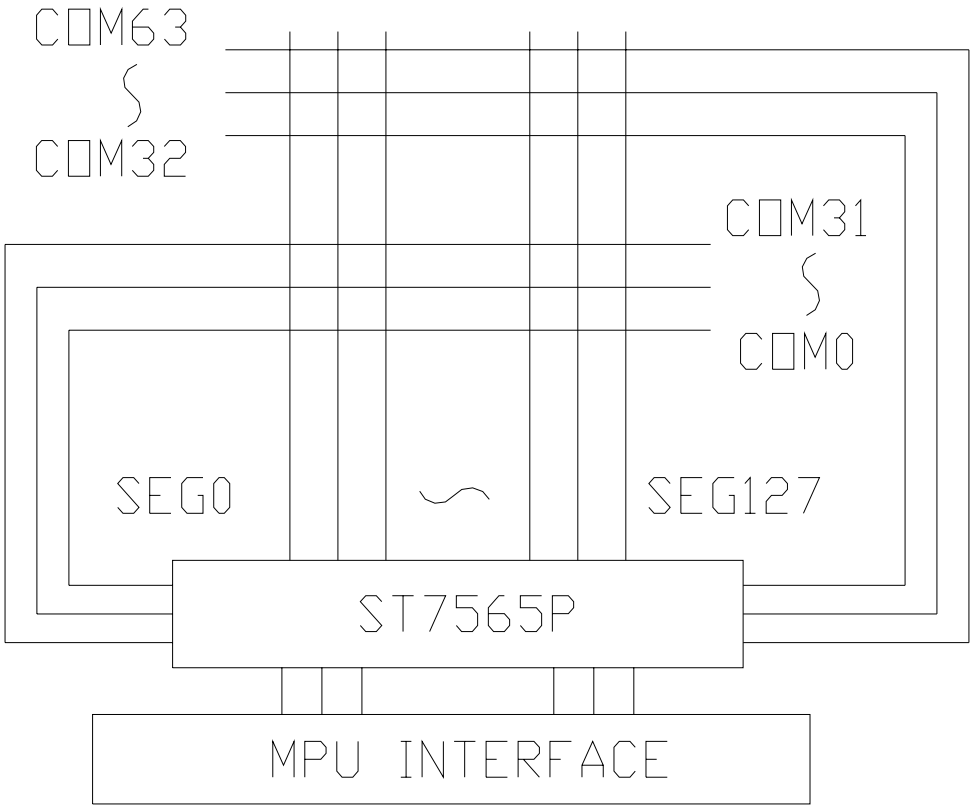
8.2 DISPLAY CONTROL INSTRUCTION

Instruction	A0	RD	WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
1.Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON /OFF, 0: OFF 1: ON
2.Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address.
3.Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address.
4.Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address
5.Status read	0	0	1	Status				0	0	0	0	Reads the status data
6.Display data write	1	1	0	Write data								Writes to the display RAM
7.Display data read	1	0	1	Read data								Reads from the display RAM
8.ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence. 0: normal 1: reverse
9.Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0: normal 1: reverse

10.Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
11. LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD driver voltage bias. 0:1/9 1: 1/7
12.Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
13.End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
14.Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
15.Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
16.Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
17.V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resist or ratio (Rb /Ra) mode
18.Electronic volume mode set Electronic volume register set	0 0	1 1	0 0	1 0	0 0	0	0	0 Electronic volume value	0	0	1	Set the V_0 output voltage electronic volume register
19.Static indicator ON/OFF Static indicator register set	0 0	1 1	0 0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF 1: ON Set the flashing mode
20.Booster ratio set	0 0	1 1	0 0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	Select booster ratio 00:2×,3×,4× 01:5× 11:6×
21.Power saver												Display OFF and display all points ON compound command
22.NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
23.Test	0	1	0	1 1	1 1	1 0	1 1	* 0	* 1	* 0	* 0	Command for IC test. Do not use this command

Note: * Disabled bit.

9.DISPLAY DATA RAM ADDRESS MAP



10. RELIABILITY TEST

V_{DD}=3V Ta=25℃

Item	Condition	Standard	Note
High temp. storage	80℃,120 hrs	Appearance without defect	---
Low temp. storage	– 30℃,120 hrs	Appearance without defect	---
High temp. operation	70℃,240 hrs	Appearance without defect	---
Low temp. storage	– 20℃,240 hrs	Appearance without defect	---
High temp. & humi. storage	50℃,90% RH,120 hrs	Appearance without defect	---
High temp .& humi. operation	40℃,90% RH,120 hrs	Appearance without defect	---
Thermal shock	-20 ℃ ,30min → +25 ℃,5min→+60℃,30min	Appearance without defect	10 cycles

11. INTERNAL PIN CONNECTIONS

并行方式接口：

Pin No	Symbol	Level	Function
1	/CS	L	Chip select signal
2	/RES	L	Reset signal
3	A0	H/L	H: DB0-DB7 are display control data L: DB0-DB7 are display data
4	/WR (R/W)	L	When 8080 MPU /WR→L When 6800 series MPU R/W→H：read R/W→L: write
5	/RD (E)	L	When 8080 MPU /RD→L When 6800 series MPUE→H
6	DB0	H/L	Data bit 0
7	DB1	H/L	Data bit 1
8	DB2	H/L	Data bit 2
9	DB3	H/L	Data bit 3
10	DB4	H/L	Data bit 4
11	DB5	H/L	Data bit 5
12	DB6	H/L	Data bit 6
13	DB7	H/L	Data bit 7
14	VDD	3.0V-5.0V	Supply voltage for logic
15	VSS	0V	Ground
16	C86	H/L	H : 6800 series MPU interface L : 8080 MPU interface
17	P/S	H/L	H : parallel data input L : serial data input
18	*LED+	3.0-5.0V	Edge light anode

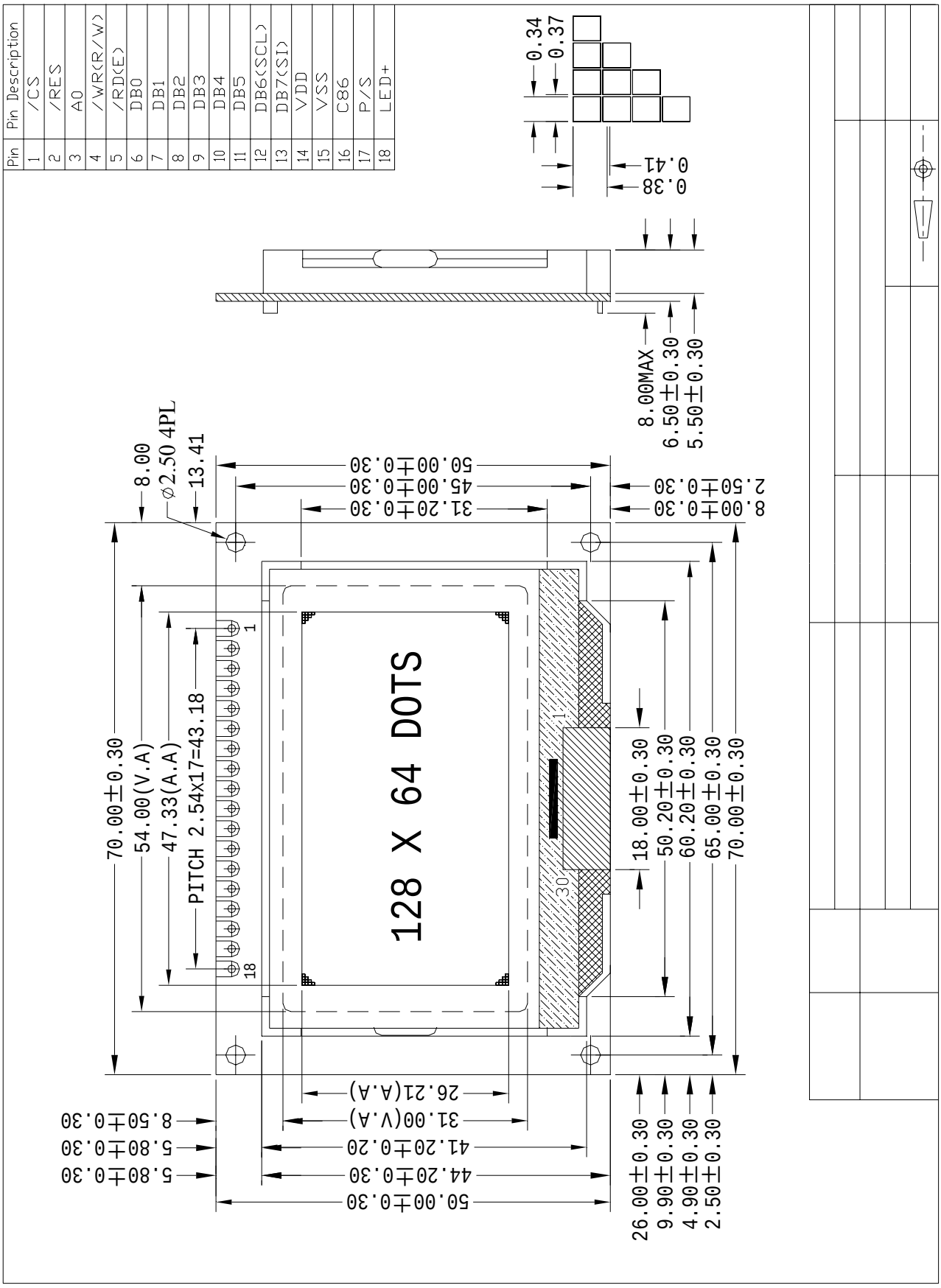
串行方式接口：

1	/CS	L	Chip select signal
2	/RES	L	Reset signal
3	A0	H/L	H: Indicates that display data exists in bits SI, and SCL. L: Indicates that display control commands exist in bits SI, and SCL.
12	SCL	H/L	the serial clock input
13	SI	H/L	serial data input
14	VDD	3.0V-5.0V	Supply voltage for logic
15	VSS	0V	Ground
18	*LED+	3.0-5.0V	Edge light anode

*** LED+=5.0V, R1=R2=R3=100Ω**

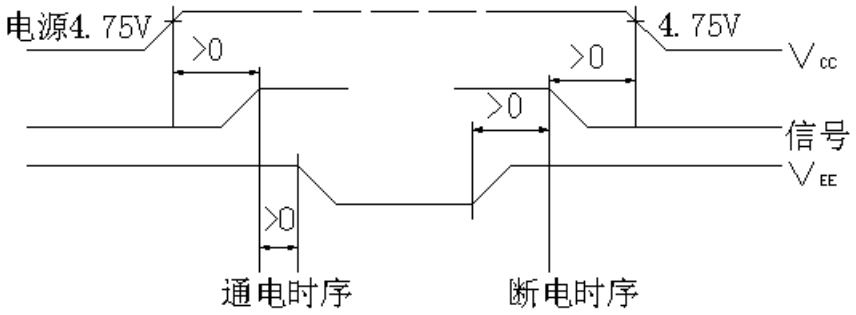
LED+=3.0V, R1=R2=R3=0Ω

12. DIMENSIONAL OUTLINE



液晶显示模块使用注意事项

1. 请勿随意自行加工、整修、拆卸。
2. 避免对液晶屏表面施加压力。
3. 不要用手随意去摸外引线、电路板上的电路及金属框。
4. 如必须直接接触时，应使人体与模块保持同一电位，或将人体良好接地。
5. 焊接使用的烙铁、操作用的电动改锥等工具必须良好接地，没漏电。
6. 严防各种静电。
7. 模块使用接入电源及断开电源时，必须按图时序进行。即必须在正电源（ 5 ±0.25V）稳定接入后,才能输入信号电平。如在电源稳定接入前，或断开后就输入信号电平，将会损坏模块中的集成电路，使模块损坏。



8. 点阵模块在调节时，应调整 VEE 至最佳对比度、视角时为止。如果 VEE 调整过高,不仅会影响显示，还会缩短液晶的寿命。
9. 模块表面结雾时，不要通电工作，因为这将引起电极化学反应，产生断线。
10. 模块要存储在暗处（避阳光），温度在-10℃～+35℃，湿度在 RH60%以上的地方。如能装入聚乙烯口袋（最好有防静电涂层）并将口封住最好。

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服务电话：010-52926620,82626833

公司地址：北京市中关村大街 32 号蓝天和盛大厦 811 室