中显液晶
技术资料

中显控制器使用说明书

2009年3月15日

北京市海淀区中关村大街32号和盛大厦811室
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企业网站：http://www.zxlcd.com

Sitronix

ST7588

81 x 132 Dot Matrix LCD Controller/Driver

n INTRODUCTION

The ST7588 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 132 segment and 80 common+1ICON driver circuits. This chip is connected directly to a microprocessor, accepts 3-line serial peripheral interface (SPI), 4-line serial peripheral interface (SPI), I^2C interface or 8-bit parallel interface, display data can stores in an on-chip display data RAM of 81 x 132 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

n FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

132 segment outputs / 81 common outputs

On-chip Display Data ram

- Capacity: 81X132=10,692 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line A mode SPI (write only)
- 4-line B mode SPI (write only)
- 3-line 8 bit A mode SPI (write only)
- 3-line 8 bit B mode SPI (write only)
- 3 line 9 bit SPI (write only)
- I^2C (Inter-Integrated Circuit) Interface (write only)

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally Vout voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components (external clock also possible)
- Voltage converter (x2, x3, x4, x5, x6)
- Voltage regulator(temperature gradient -0.1%/°C)
- Voltage follower
- On-chip electronic contrast control function (128 steps)

External RESB (reset) pin

Logic supply voltage range $V_{DD1,2}$ -V_{SS}

- 1.8 to 3.3V

Display supply voltage range V_{LCD} -V_{SS}

- 4.5 to 13V

Temperature range: -40 to +85 degree

ST7588	**6800, 8080, 4-Line, 3-Line interface (without I^2C interface)**	
ST7588i	**I^2C interface**	

n PAD Arrangement (COG)

Chip Size: 7,708 μm ×980μm

Bump Pitch:

PAD NO 1~185, 248~276: 45 μm (com/seg)

PAD NO 186~187, 188~189, 191~192, 193~194, 195~196, 197~198, 199~200, 201~202, 213~214,215~216: 119 μm

PAD NO 187~188, 189~190, 192~193, 194~195, 196~197, 198~199, 200~201, 209~211, 212~213, 214~215, 216~217, 218~220: 73μm

PAD NO 190~191: 134 μm PAD NO 202~203: 77μm; PAD NO 204~205, 206~207: 75μm

PAD NO 203~204, 205~206: 175 μm; PAD NO 207~208: 150μm; PAD NO 211~212, 217~218: 102 μm

PAD NO 220~221: 93μm; PAD NO 208~209: 68μm; PAD NO 221~243, 244~247: 70μm; PAD 243~244: 145μm

Bump Size:

PAD NO 1~156, 174~185, 248~259: 30(x) μm × 80(y) μm

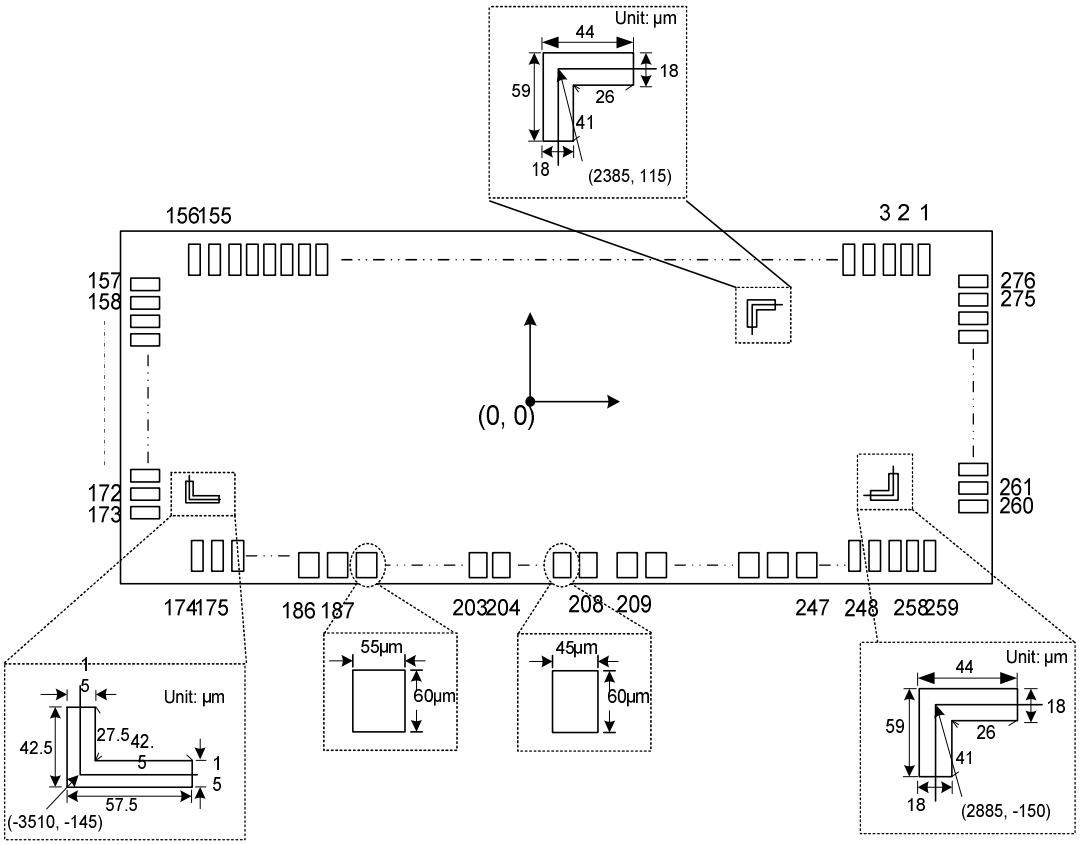
PAD NO 157~173, 260~276: 80(x) μm × 30(y) μm

PAD NO 186 ~ 202, 209 ~ 247 : 55(x)μm × 60(y) μm

PAD NO 203~208: 45(x) μm × 60(y) μm

Bump Height: 17±3μm (Typ)

Chip Thickness: 482.6 μm



n Pad Center Coordinates (49 duty)

Pad No.	Pin Name	X	Y
001	none	3487	379
002	none	3442	379
003	none	3397	379
004	none	3352	379
005	none	3307	379
006	none	3262	379
007	none	3217	379
008	none	3172	379
009	none	3127	379
010	none	3082	379
011	none	3037	379
012	none	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	none	-3743	-227
171	none	-3743	-272
172	none	-3743	-317
173	none	-3743	-362
174	none	-3488	-379
175	none	-3443	-379
176	none	-3398	-379
177	none	-3353	-379
178	none	-3308	-379

Pad No.	Pin Name	X	Y
179	none	-3263	-379
180	none	-3218	-379
181	none	-3173	-379
182	none	-3128	-379
183	none	-3083	-379
184	none	-3038	-379
185	none	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	TM	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	VDD	782	-389
219	VDD	855	-389
220	VDD	928	-389
221	VDD2	1021	-389
222	VDD2	1091	-389
223	VOUT	1161	-389
224	VOUT	1231	-389
225	VOUT	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389

Pad No.	Pin Name	X	Y
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[47]	3037	-379
250	COM[46]	3082	-379
251	COM[45]	3127	-379
252	COM[44]	3172	-379
253	COM[43]	3217	-379
254	COM[42]	3262	-379
255	COM[41]	3307	-379
256	COM[40]	3352	-379
257	COM[39]	3397	-379
258	COM[38]	3442	-379
259	COM[37]	3487	-379
260	COM[36]	3743	-362
261	COM[35]	3743	-317
262	COM[34]	3743	-272
263	COM[33]	3743	-227
264	COM[32]	3743	-182
265	COM[31]	3743	-137
266	COM[30]	3743	-92
267	COM[29]	3743	-47
268	COM[28]	3743	-2
269	COM[27]	3743	43
270	COM[26]	3743	88
271	COM[25]	3743	133
272	COM[24]	3743	178
273	none	3743	223
274	none	3743	268
275	none	3743	313
276	none	3743	358

n Pad Center Coordinates (65 duty)

Pad No.	Pin Name	X	Y
001	COM[35]	3487	379
002	COM[34]	3442	379
003	COM[33]	3397	379
004	COM[32]	3352	379
005	none	3307	379
006	none	3262	379
007	none	3217	379
008	none	3172	379
009	none	3127	379
010	none	3082	379
011	none	3037	379
012	none	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	COM[24]	-3743	-227
171	COM[25]	-3743	-272
172	COM[26]	-3743	-317
173	COM[27]	-3743	-362
174	COM[28]	-3488	-379
175	COM[29]	-3443	-379
176	COM[30]	-3398	-379
177	COM[31]	-3353	-379
178	none	-3308	-379

Pad No.	Pin Name	X	Y
179	none	-3263	-379
180	none	-3218	-379
181	none	-3173	-379
182	none	-3128	-379
183	none	-3083	-379
184	none	-3038	-379
185	none	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	TM	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	VDD	782	-389
219	VDD	855	-389
220	VDD	928	-389
221	VDD2	1021	-389
222	VDD2	1091	-389
223	VOUT	1161	-389
224	VOUT	1231	-389
225	VOUT	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389

Pad No.	Pin Name	X	Y
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[63]	3037	-379
250	COM[62]	3082	-379
251	COM[61]	3127	-379
252	COM[60]	3172	-379
253	COM[59]	3217	-379
254	COM[58]	3262	-379
255	COM[57]	3307	-379
256	COM[56]	3352	-379
257	COM[55]	3397	-379
258	COM[54]	3442	-379
259	COM[53]	3487	-379
260	COM[52]	3743	-362
261	COM[51]	3743	-317
262	COM[50]	3743	-272
263	COM[49]	3743	-227
264	COM[48]	3743	-182
265	COM[47]	3743	-137
266	COM[46]	3743	-92
267	COM[45]	3743	-47
268	COM[44]	3743	-2
269	COM[43]	3743	43
270	COM[42]	3743	88
271	COM[41]	3743	133
272	COM[40]	3743	178
273	COM[39]	3743	223
274	COM[38]	3743	268
275	COM[37]	3743	313
276	COM[36]	3743	358

n Pad Center Coordinates (81 duty)

Pad No.	Pin Name	X	Y
001	COM[51]	3487	379
002	COM[50]	3442	379
003	COM[49]	3397	379
004	COM[48]	3352	379
005	COM[47]	3307	379
006	COM[46]	3262	379
007	COM[45]	3217	379
008	COM[44]	3172	379
009	COM[43]	3127	379
010	COM[42]	3082	379
011	COM[41]	3037	379
012	COM[40]	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	COM[24]	-3743	-227
171	COM[25]	-3743	-272
172	COM[26]	-3743	-317
173	COM[27]	-3743	-362
174	COM[28]	-3488	-379
175	COM[29]	-3443	-379
176	COM[30]	-3398	-379
177	COM[31]	-3353	-379
178	COM[32]	-3308	-379

Pad No.	Pin Name	X	Y
179	COM[33]	-3263	-379
180	COM[34]	-3218	-379
181	COM[35]	-3173	-379
182	COM[36]	-3128	-379
183	COM[37]	-3083	-379
184	COM[38]	-3038	-379
185	COM[39]	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	TM	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	VDD	782	-389
219	VDD	855	-389
220	VDD	928	-389
221	VDD2	1021	-389
222	VDD2	1091	-389
223	VOUT	1161	-389
224	VOUT	1231	-389
225	VOUT	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[79]	3037	-379
250	COM[78]	3082	-379

Pad No.	Pin Name	X	Y
251	COM[77]	3127	-379
252	COM[76]	3172	-379
253	COM[75]	3217	-379
254	COM[74]	3262	-379
255	COM[73]	3307	-379
256	COM[72]	3352	-379
257	COM[71]	3397	-379
258	COM[70]	3442	-379
259	COM[69]	3487	-379
260	COM[68]	3743	-362
261	COM[67]	3743	-317
262	COM[66]	3743	-272
263	COM[65]	3743	-227
264	COM[64]	3743	-182
265	COM[63]	3743	-137
266	COM[62]	3743	-92
267	COM[61]	3743	-47
268	COM[60]	3743	-2
269	COM[59]	3743	43
270	COM[58]	3743	88
271	COM[57]	3743	133
272	COM[56]	3743	178
273	COM[55]	3743	223
274	COM[54]	3743	268
275	COM[53]	3743	313
276	COM[52]	3743	358

n BLOCK DIAGRAM

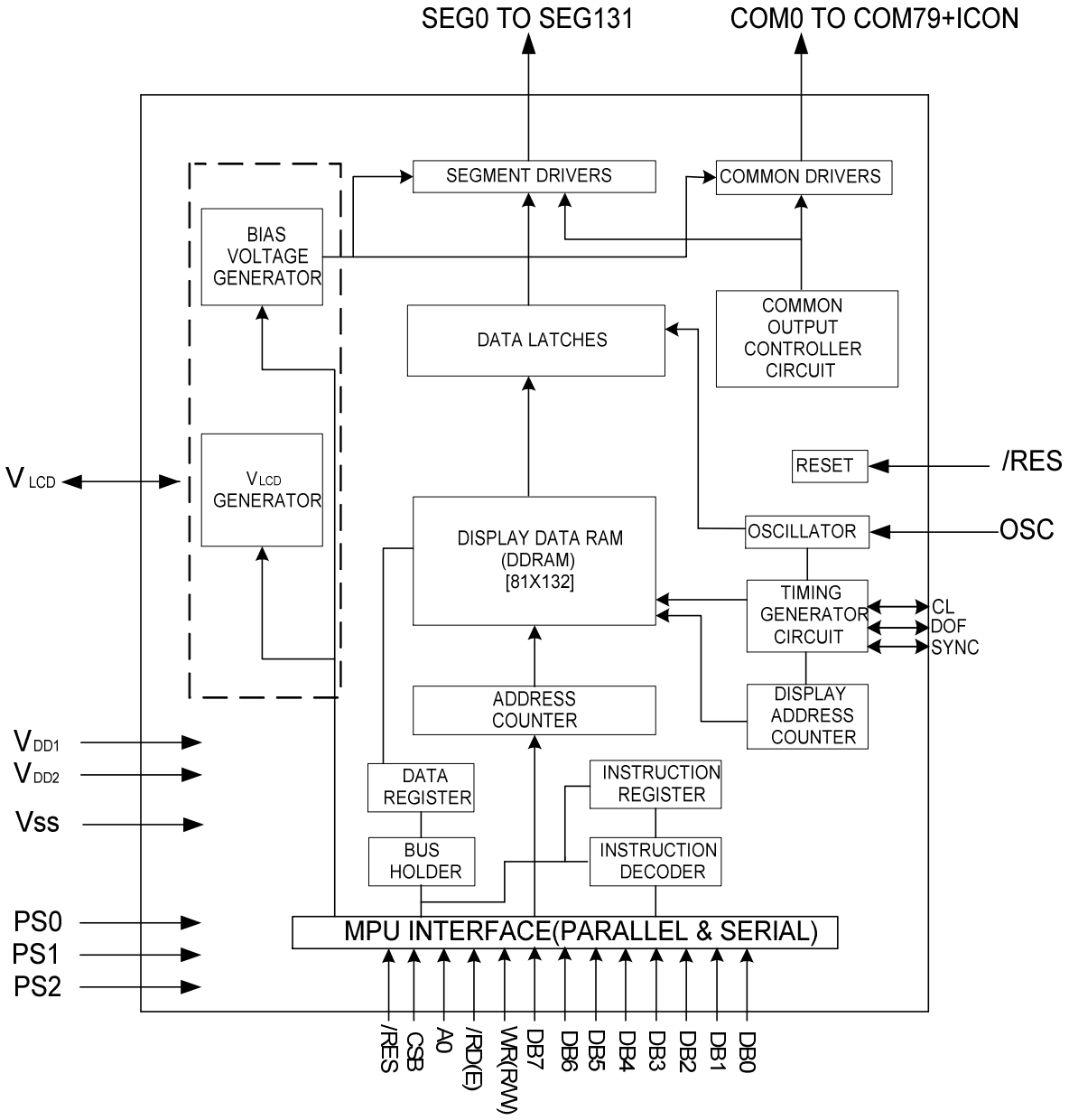


Figure 1 block diagram

n PIN DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">LCD driver outputs</td></tr>
<tr><td>SEG0 to SEG131</td><td>O</td><td>LCD segment driver outputs
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0 to COM79</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M(Internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V_0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V_1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V_4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>80</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface select input pin
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>State</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4-line serial interface A mode</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-line serial interface B mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3-line (8 bit) serial interface A mode</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-line (8-bit) serial interface B mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3-line (9-bit) serial interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IIC serial interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 is high impedance.
There is no CSB pin in I^2C interface, so this pin can fix to ” H”</td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESB is "L", initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H “: Indicates that D0 to D7 are display data.
A0=" L “: Indicates that D0 to D7 are control data.
There is no A0 pin in three line or I^2C interface, so this pin can fix to ” H”</td><td>1</td></tr>
</table>

<table>
<tr><td>/WR(R/W)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>PS2</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=" H ": read
R/W=" L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal</td></tr>
</table>
When in the serial interface must fix to ” H”</td><td>1</td></tr>
<tr><td>/RD (E)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>PS2</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=" H ": When E is " H ", D0 to D7 are in an output status.
R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is "L", D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface must fix to ” H”</td><td>1</td></tr>
<tr><td>D7 to D4
D1 to D3 (SDA)
D0 (SCL)</td><td rowspan="2">I/O</td><td>When the parallel interface selected: 8-bit interface
This is an 8-bit bi-directional data bus that connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.</td><td rowspan="2">8</td></tr>
<tr><td>When the serial interface selected: 3 or 4-line
D0: serial input clock (SCL)
D1 to D3: serial input data (SDA)
D4, D5, D6, D7 : must fix to ” H”
When chip select is not active, D0 to D7 is high impedance.</td></tr>
<tr><td>D7 to D6 (SA)
D2 to D5
(SDA_OUT)
D1 (SDA_IN)
D0 (SCL)</td><td>When the serial interface selected (PS2~0="H"): I^{2}C
D0: serial clock input (SCL)
D1: serial input data (SDA_IN)
D2 to D5: (SDA_OUT) serial data acknowledge for the I^{2}C interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^{2}C interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. Due to the track resistance from the SDA_OUT pad to the system SDA line can be significant in COG application, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible that during the acknowledge cycle the ST7588 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
D6 and D7 are slave address bit 0, 1 and can be set as 00 to 11.
<u>D1 to D5 must be connected together (SDA)</u>
Chip select input pin “CSB” is not used and must be fixed to “H”</td></tr>
<tr><td>MODE0, MODE1</td><td>I</td><td>Use this pin can select 49 duty, 65duty or 81 duty mode
<table>
<tr><th>Mode1</th><th>Mode0</th><th>Duty</th></tr>
<tr><td>0</td><td>0</td><td>49 duty</td></tr>
<tr><td>0</td><td>1</td><td>65 duty</td></tr>
<tr><td>1</td><td>0</td><td>---</td></tr>
<tr><td>1</td><td>1</td><td>81 duty</td></tr>
</table></td><td>1</td></tr>
</table>

TM	I	This terminal is reserved for test only. It must be fixed to high.	**1**
SYNC	O	This is the liquid crystal alternating current signal terminal.	**1**
/DOF	O	This is the LCD blanking control terminal.	**1**
CL	I/O	This is the display clock output terminal and must be floating.	
Power Supply Pins			
V_{SS}	Power Supply	Ground.	**9**
V_{DD1}	Power Supply	Digital Supply Voltage. The 2 supply rails V_{DD1} and V_{DD2} could be connected together. If Digital Option pin is high, must be this level	**5**
V_{DD2}	Power Supply	Analog Supply Voltage. The 2 supply rails V_{DD1} and V_{DD2} could be connected together.	**4**
VOUT	Power Supply	If the external voltage generator is used, an external supply voltage can be supplied using the VOUT pad as an external multiple voltage input. If the internal voltage generator is used, the VOUT must series one capacitor to V_{DD2}.	**3**
V0, V1, V2, V3, V4	Power Supply	This is a multi-level power supply for the liquid crystal. VOUT-IN ≥V0 ≥V1≥V2≥V3≥V4≥VSS	**5**
VRS	Power Supply	Monitor Voltage Regulator level, must be left open.	**1**
Test Pin			
T0~T5	T	These pins are reserved for test only.	**6**

ITO Limitations

PIN Name	**ITO Resister**
SYNC, /DOF, PS0~2, M0, M1	No Limitation
T0~5	Floating
VDD, VDD2, Vss, VRS, VOUT	<100Ω
CSB, CL, E , R/W , A0, D0~D7	<1KΩ
V0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N , CAP3P, CAP3N, CAP4P, CAP5P	<100Ω
RESB	<10KΩ

n FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7588 can interface with an MPU when CSB is "L". When these pins are set to any other combination, A0, /RD (E), and /WR(R/W) inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7588 has eight types of interface with an MPU, which are six serial and two parallel interfaces. This parallel or serial interface is determined by PS0, PS1 and PS2 pin as shown in Table 1.

Table 1 Parallel / Serial Interface Mode

Type	PS2	PS1	PS0	Interface mode
Parallel	0	0	0	8bit 8080-series MPU mode
	1	0	0	8 bit 6800-series MPU mode
Serial	0	1	0	4-line serial interface A mode
	1	1	0	4-line serial interface B mode
	0	0	1	3-line (8 bit) serial interface A mode
	1	0	1	3-line (8-bit) serial interface B mode
	0	1	1	3-line (9-bit) serial interface
	1	1	1	IIC serial interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS0 as shown in Table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS2	CSB	A0	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	A0	E	RW	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, the interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, RW_WR as in case of 6800-series mode.

Serial Interface

4-Line SPI

When the ST7588 is active (CSB=”L”), serial data (DB1~3) and serial clock (DB0) inputs are enabled. While not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either by software or the Register Select (A0) Pin. When the A0 pin is used, data is display data when A0 is high, and command data when A0 is low. When A0 is not used, the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command (11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sent, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

n 4-Line SPI A Mode (PS0 = "L", PS1 = "H" , PS2 = "L")

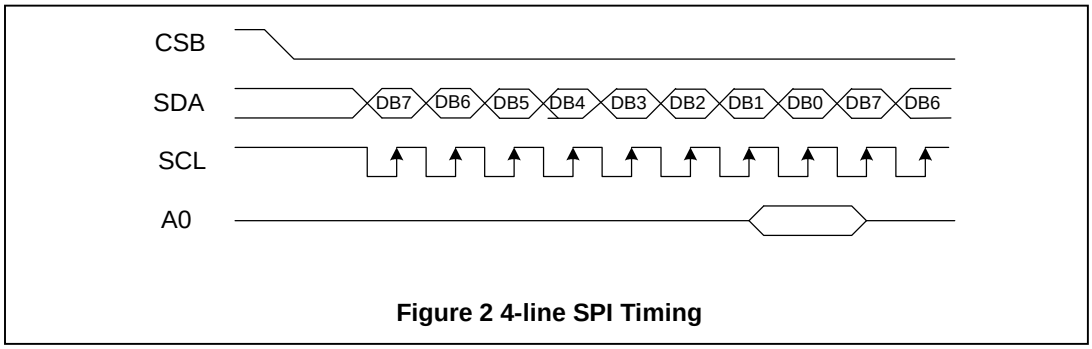


Figure 2 4-line SPI Timing

n 4-Line SPI B Mode (PS0 = "L", PS1 = "H" , PS2 = "H")

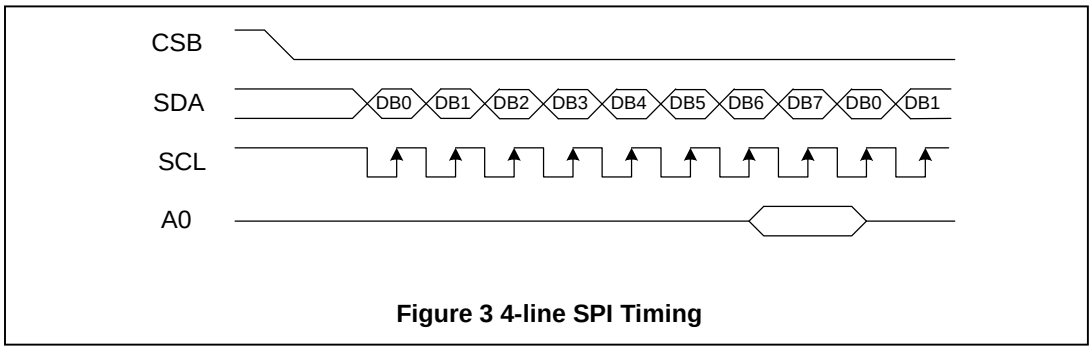
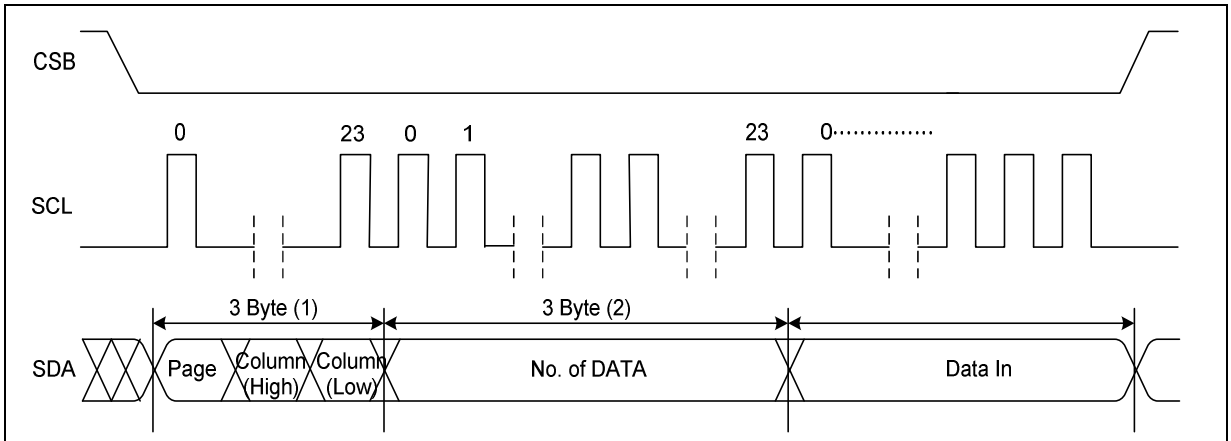


Figure 3 4-line SPI Timing

3-Line SPI

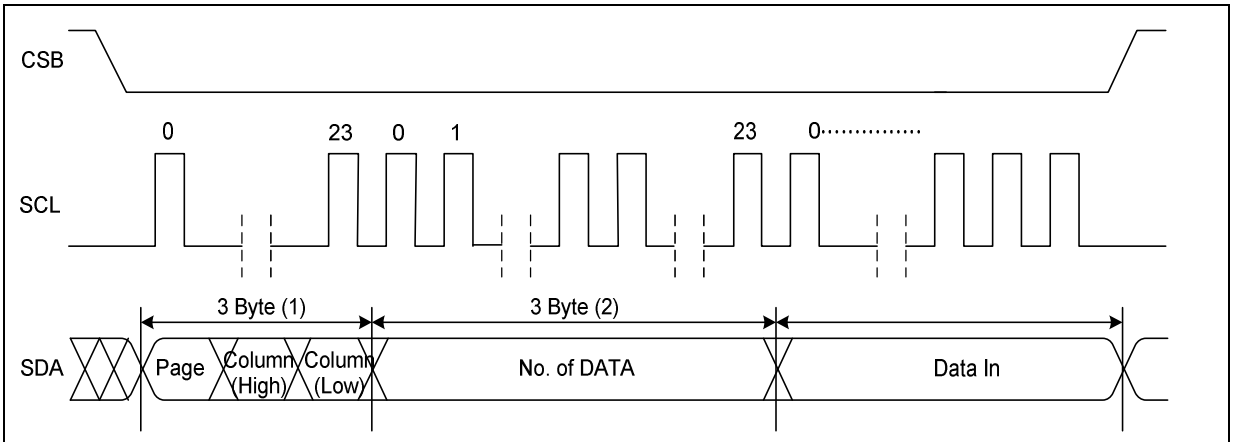
n 3-Line SPI (8 bit)

To write data to the DDRAM, set address and No. of Data Bytes before transferring data, then data will be latched at the rising edge of SCL. The DDRAM column address pointer will be increased by one automatically.



1. Set Page Address:	0	1	0	0	Y3	Y2	Y1	Y0
Set Column Address (High):	1	1	1	1	X7	X6	X5	X4
Set Column Address (Low):	1	1	1	0	X3	X2	X1	X0
2. Set No. of Data Bytes (M):	0	1	1	1	0	DA10	DA9	DA8
Set No. of Data Bytes (L):	0	1	1	0	DA7	DA6	DA5	DA4
Set No. of Data Bytes & Start	0	1	0	1	DA3	DA2	DA1	DA0
3. Transfer Data bytes.								

Figure 4 3-pin SPI (8 bit) A mode Timing (A0 is not used)



1. Set Page Address:	Y0	Y1	Y2	Y3	0	0	1	0
Set Column Address (High):	X4	X5	X6	X7	1	1	1	1
Set Column Address (Low):	X0	X1	X2	X3	0	1	1	1
2. Set No. of Data Bytes (M):	DA8	DA9	DA10	0	1	1	1	0
Set No. of Data Bytes (L):	DA4	DA5	DA6	DA7	0	1	1	0
Set No. of Data Bytes & Start	DA0	DA1	DA2	DA3	1	0	1	0
3. Transfer Data bytes.								

Figure 5 3-pin SPI (8 bit) B mode Timing (A0 is not used)

This command is used in 3-Line SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is halted in transmitting, it is not valid data.
New data will be transferred serially with most significant bit first.
NOTE: In spite of transmission of data, if CSB is disabled, state stops abnormally. Next state is initialized.

n 3-Line SPI (9 bit)

In 3-Line mode, default message from MCU is command, the 2 bytes command of Set **Data Direction & Display Data Length** must be set before display data send from MCU, after the display data is sent over, the next message is turned to be command.

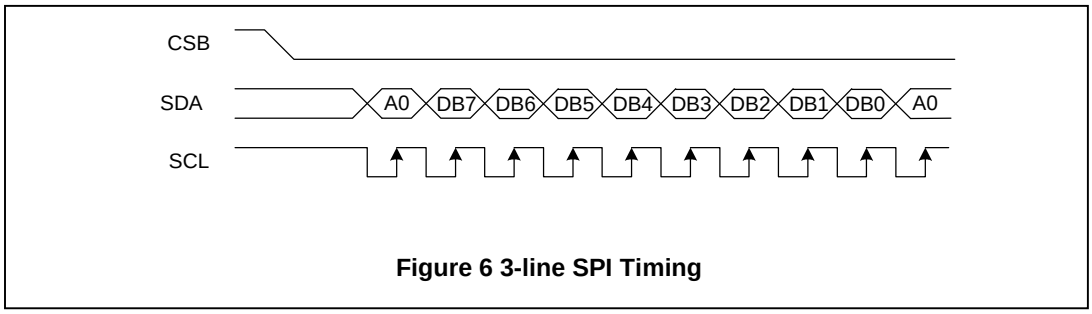


Figure 6 3-line SPI Timing

IIC Interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be regarded as a control signal. Bit transfer is illustrated in Figure 7.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 8.

SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 9.
· Transmitter: the device that sends the data to the bus.
· Receiver: the device that receives the data from the bus.
· Master: the device that initiates transmission, generates clock signals, and terminates a transfer.
· Slave: the device addressed by a master.
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. A master receiver must also generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledgement related clock pulse (set-up and hold times must be taken into consideration). A

master receiver must signal an end-of-data to the transmitter by not generating an acknowledgement on the last byte that has been clocked out of the slave. In this situation, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Figure 10.

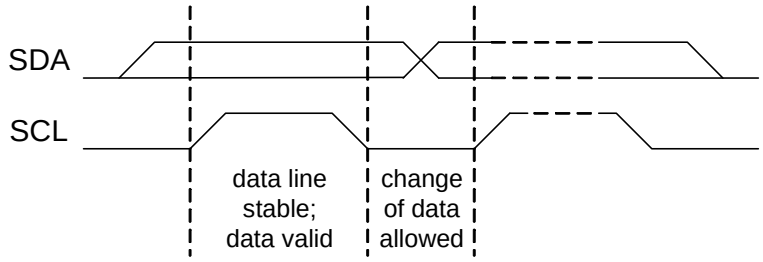


Figure 8 Bit transfer

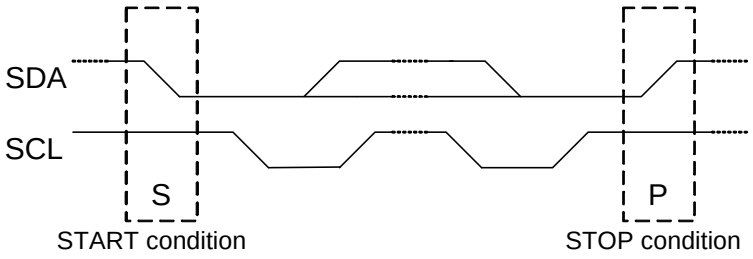


Figure 9 Definition of START and STOP conditions

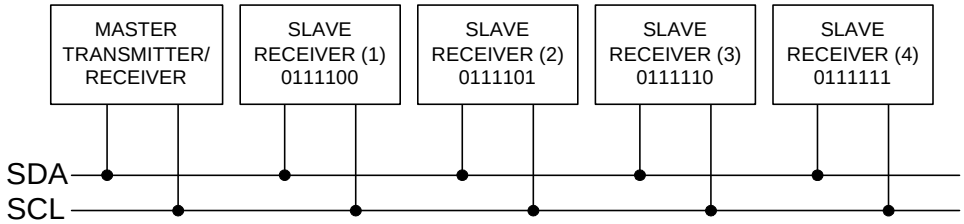


Figure 10 System configuration

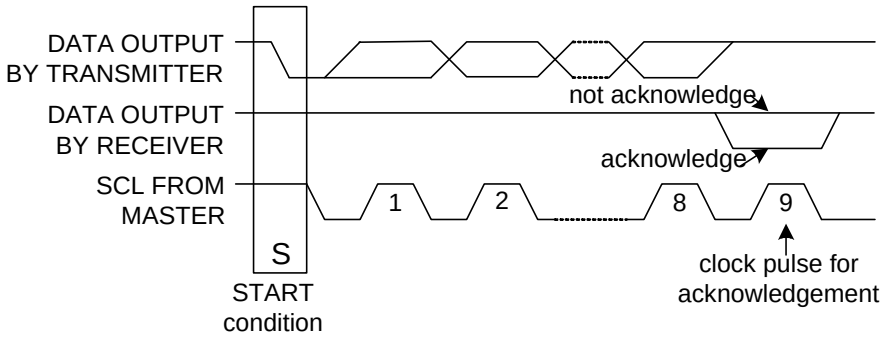


Figure 7 Acknowledgement on the 2-line Interface

IIC Interface protocol

The ST7588 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110, and 0111111) are reserved for the ST7588. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (V_{SS}) or logic 1 (V_{DD}).
The IIC Interface protocol is illustrated in Figure 11.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is regarded as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7588 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If the master generates no acknowledgement after a byte, the driver stops transferring data to the master.

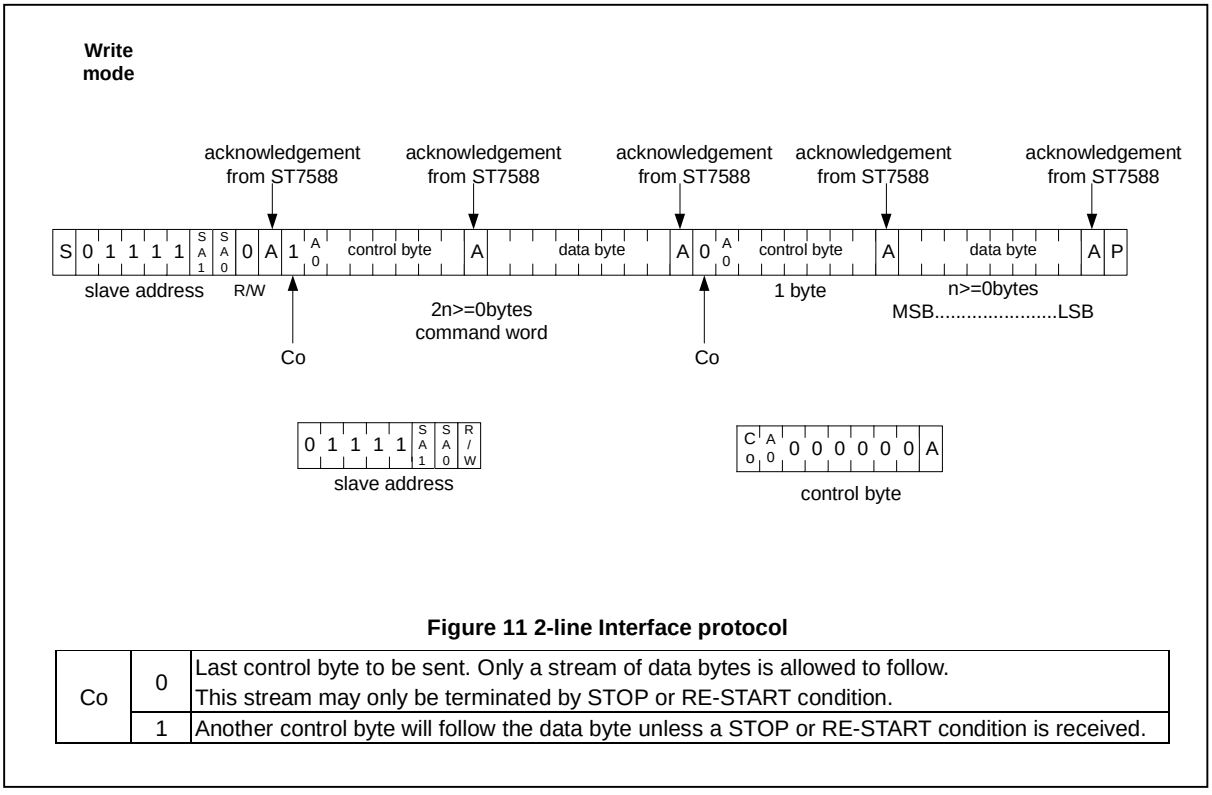


Figure 11 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Busy Flag

The Busy Flag indicates whether the ST7588 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The ST7588 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 12. Moreover, when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 13. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

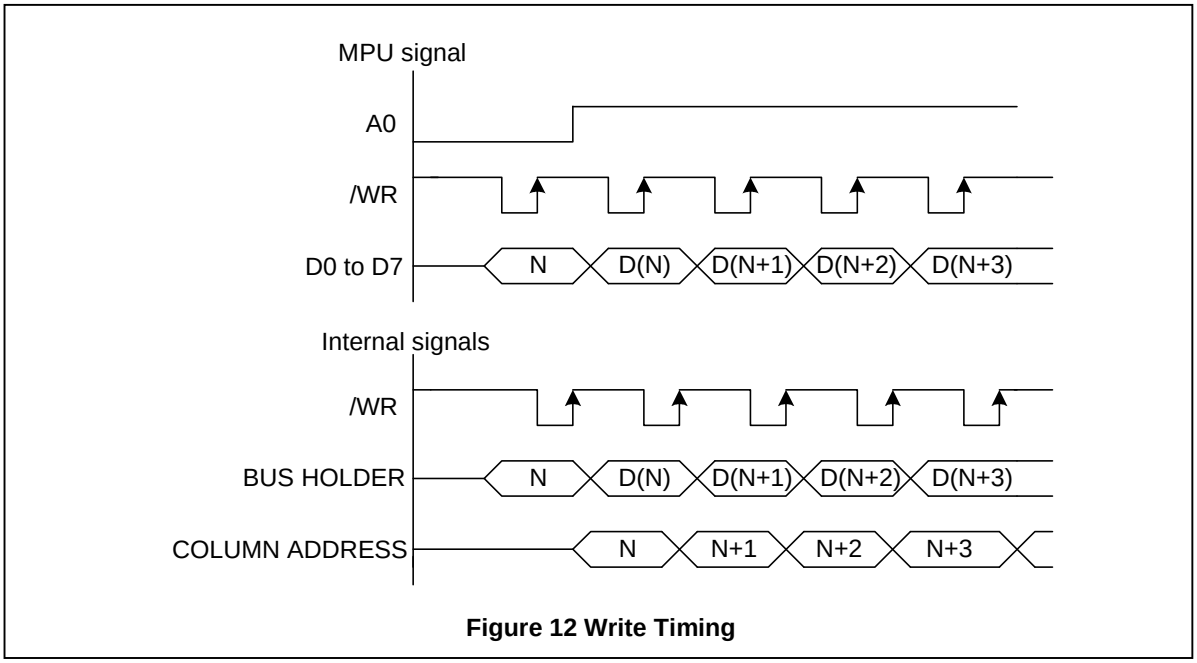


Figure 12 Write Timing

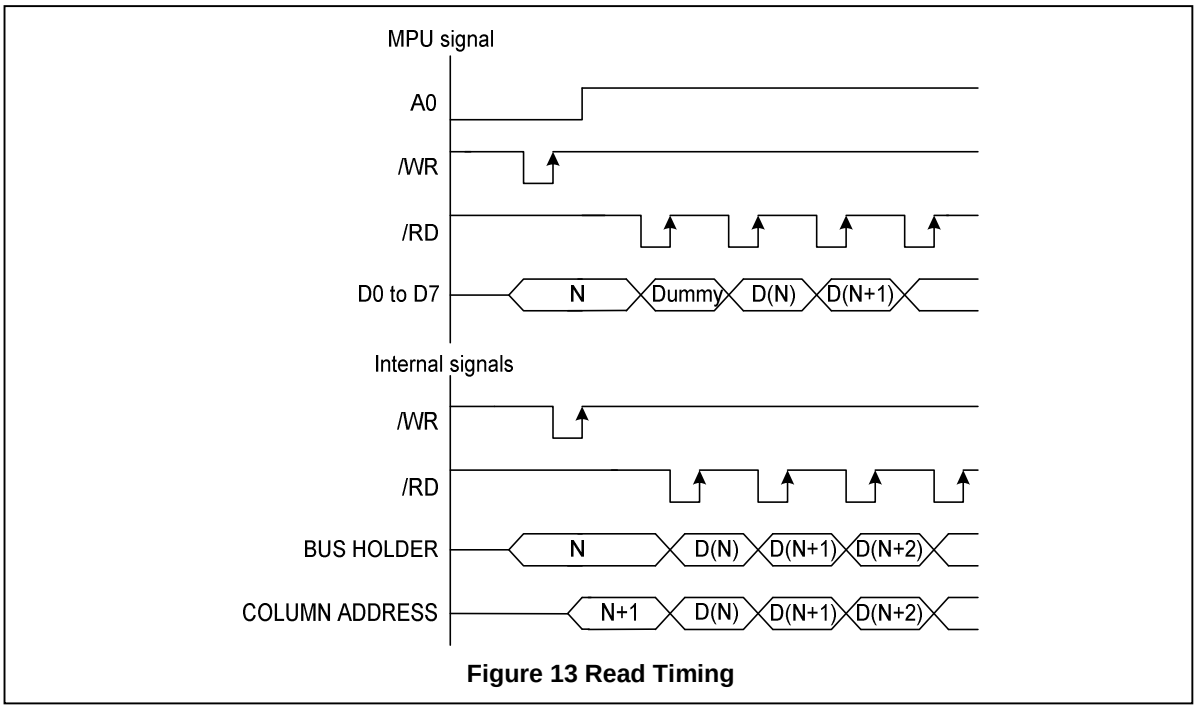


Figure 13 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7588 contains a 81X132 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 81(10 pageX8 bit +1 pageX1 bit) X 132. There is a direct correspondence between X-address and column output number. It is 81-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 11 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 132-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in Figure 14. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction. Refer to the following Figure 15.

SEG Output

SEG Output MX	SEG0 SEG131
"0"	seg0 **à** Segment Address **à** seg131
"1"	seg131 **ß** Segment Address **ß** seg0

Com Output

SEG Output MY	Com0 Com79	Coms
"0"	com0 **à** Common Address **à** com79	Coms
"1"	Com79 **ß** Common Address **ß** com0	Coms

Data is downloaded in bytes into the RAM matrix of ST7588 as indicated in Figs.14, 15, 16. The display RAM has a matrix of 81 by 132 bits. The address pointer addresses the columns. The address ranges are as follows. X: 0 to 131 (10000011), Y: 0 to 10 (1010) .Addresses outside these ranges are not allowed.

In horizontal addressing mode, the X address increments after each byte (see Figure 16). After the last X address (X = 131) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 131, Y = 10) the address pointers wrap around to address (X = 0, Y =0)

Data structure

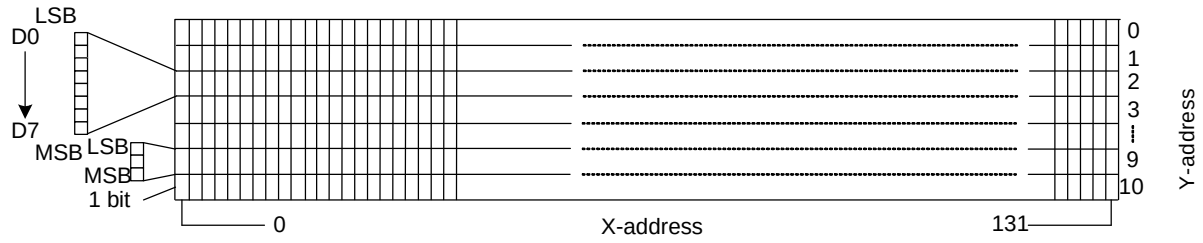


Figure 14 RAM format, addressing , if DO=0

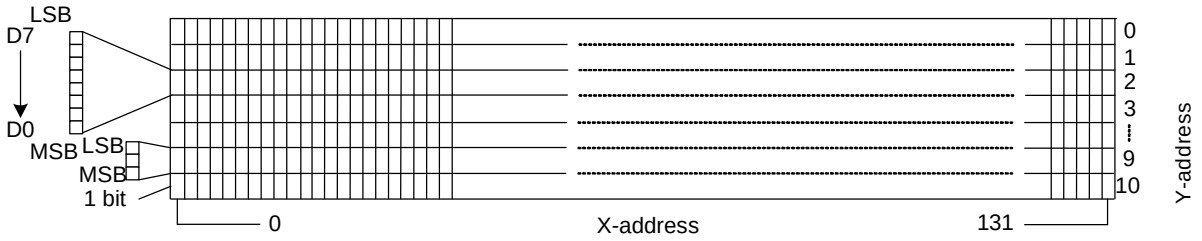


Figure 15 RAM format, addressing, if DO=1

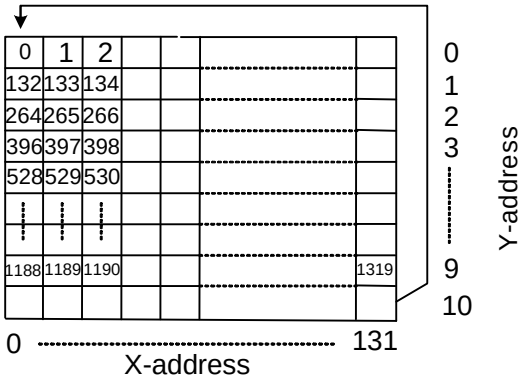
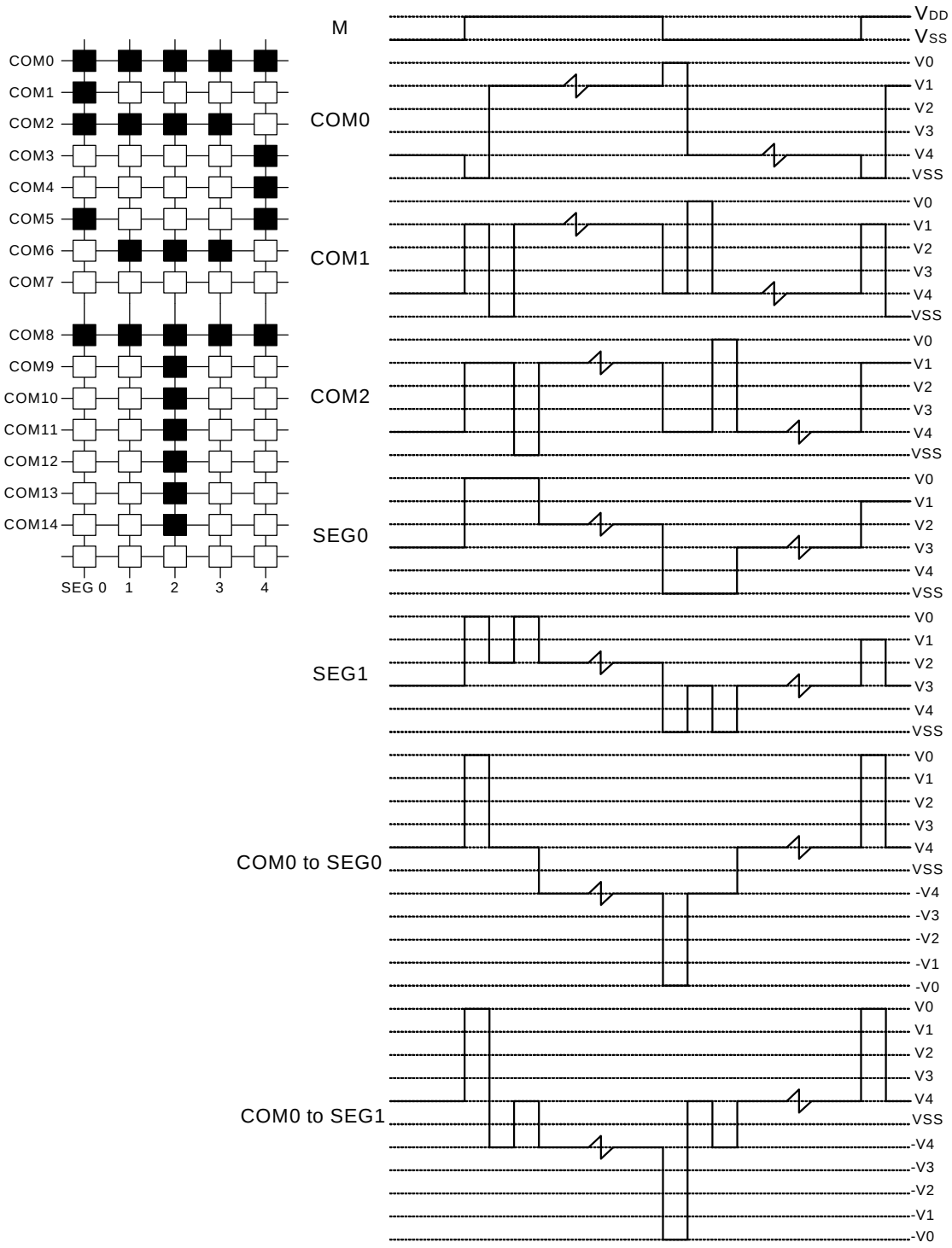


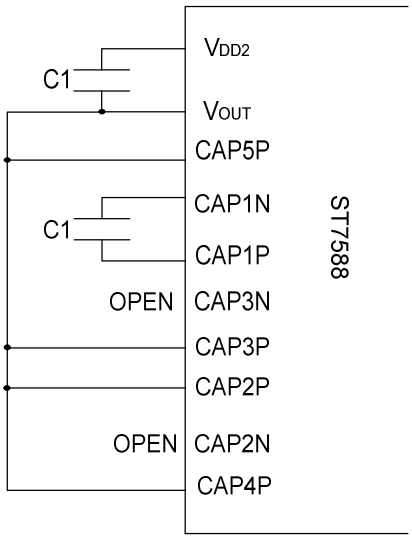
Figure 16 sequence of writing data bytes into RAM with horizontal addressing

LCD DRIVER CIRCUIT

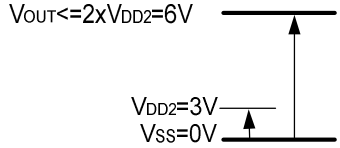
This driver circuit is configured by 81-channel common drivers and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



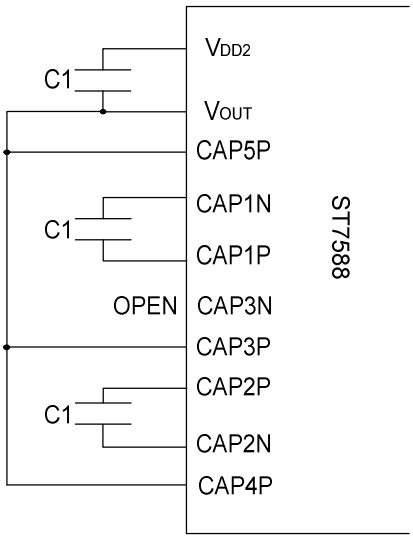
REFERENCE CIRCUIT EXAMPLE



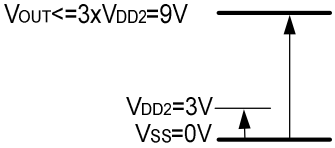
2x step-up voltage circuit



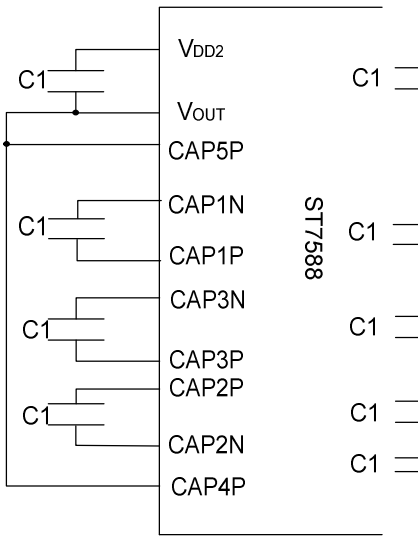
2x step-up voltage relationships



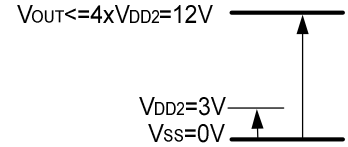
3x step-up voltage circuit



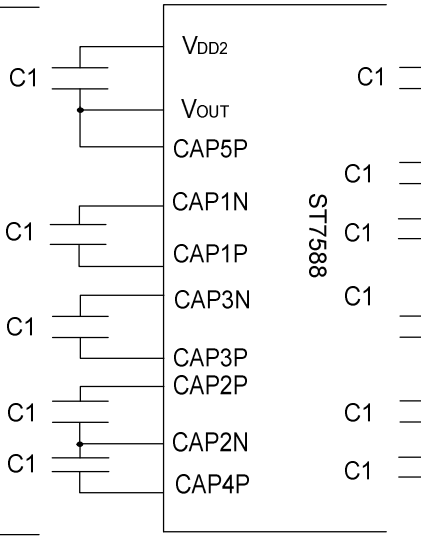
3x step-up voltage relationships



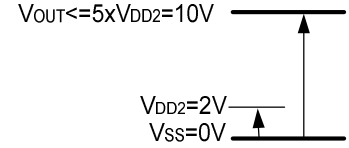
4x step-up voltage circuit



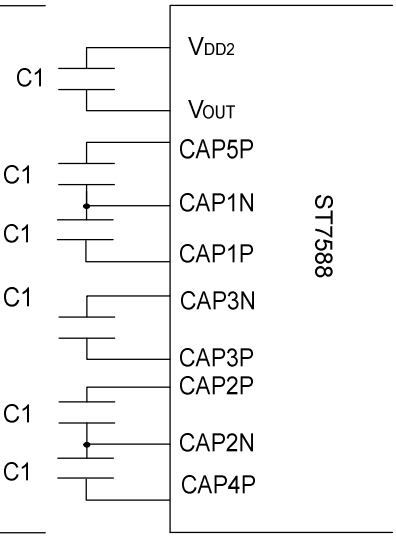
4x step-up voltage relationships



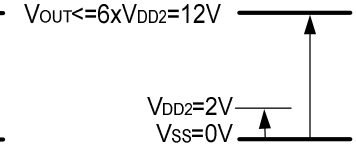
5x step-up voltage circuit



5x step-up voltage relationships



6x step-up voltage circuit



6x step-up voltage relationships

RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.
When RESB becomes “L”, the following procedure is entered.
Page address: 0
Column address: 0
Display control: Display blank
COM Scan Direction MY: 0
SEG Select Direction MX: 0
DO=0
Oscillator: OFF
N-line inversion register: 0 (disable)
Power down mode (PD = 1)
Normal instruction set (H[1:0] = 00)
Display blank (E = D = 0)
Address counter X [7:0] = 0, Y [3:0] = 0
Bias system (BS [2:0] = 0)
VLCD is equal to 0; the HV generator is switched off (VOP [6:0] = 0)
After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB0. After DB0 becomes ”L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

Partial Display on LCD

The ST7588 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

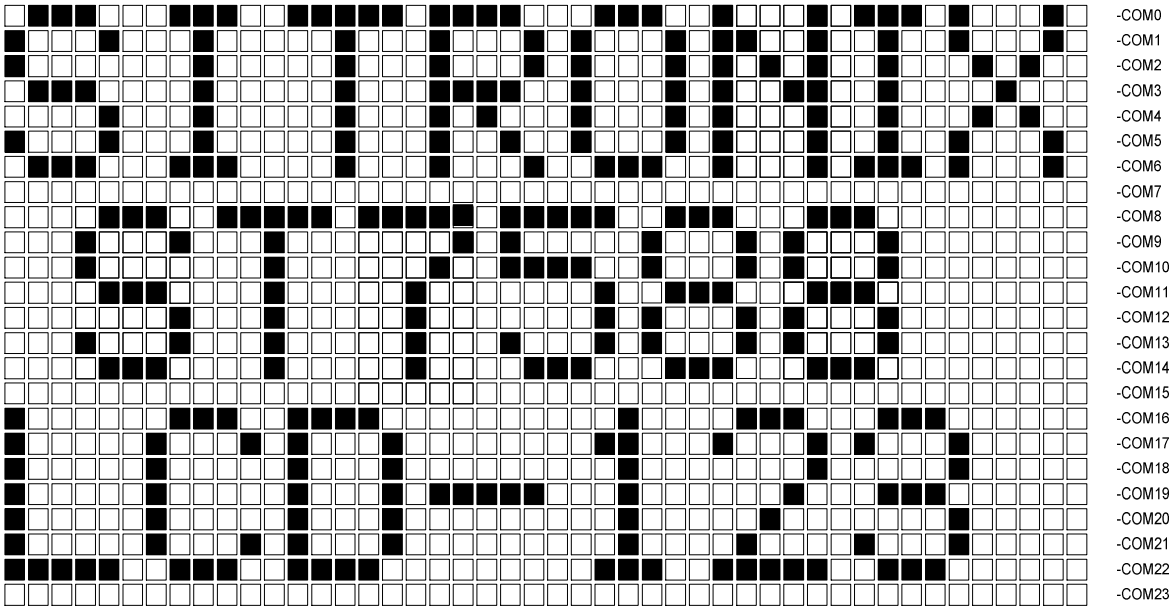


Figure 20.Reference Example for Partial Display

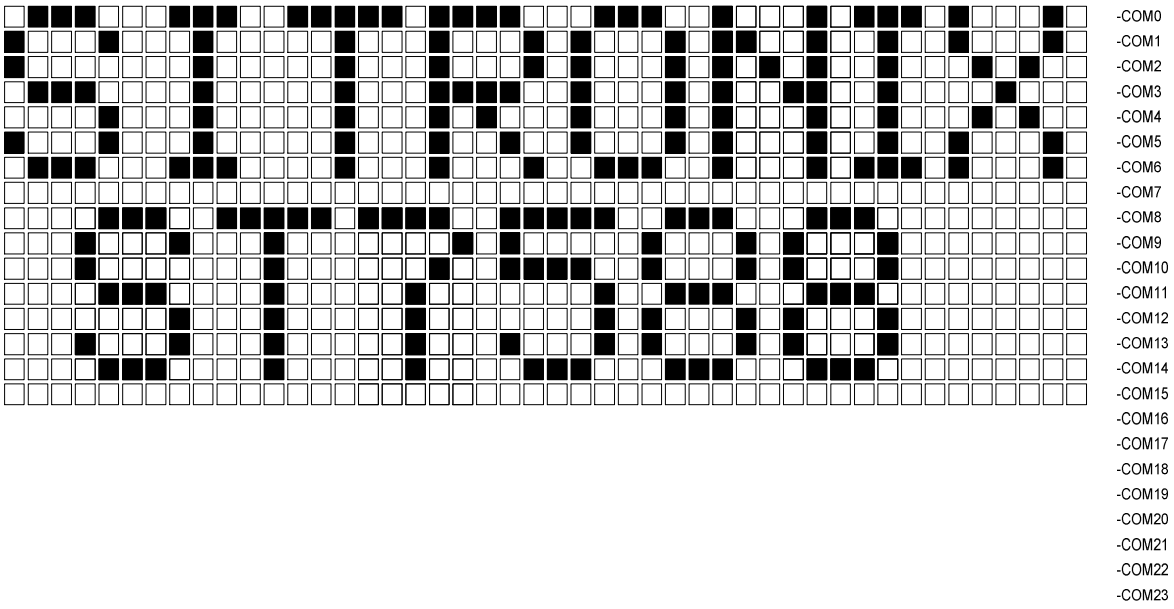


Figure 21.Partial Display (Partial Display Duty=16, initial COM0=0)

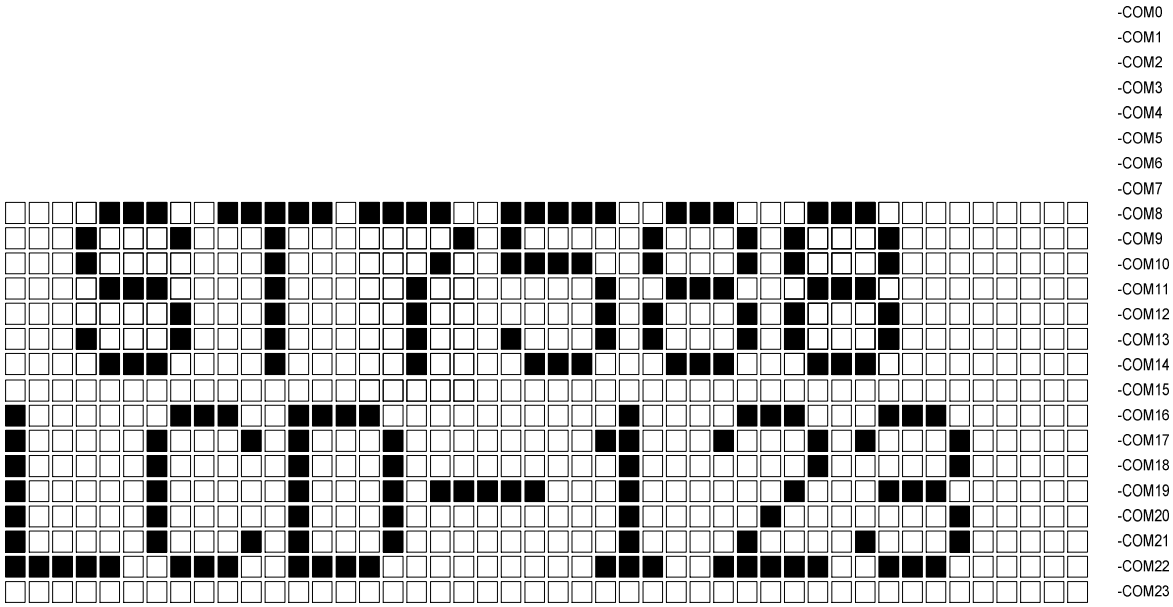


Figure 22.Moving Display (Partial Display Duty=16,Initial COM0=8)

n INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
H independent instruction											
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data to RAM
Read data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Read data to RAM
Read status byte	0	1	PD	0	V	D	E	MX	MY	DO	Read status byte
Function Set	0	0	0	0	1	MX	MY	PD	H1	H0	Mirror X, mirror Y, Power down, Extended table

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
H[1:0]=[0:0]											
Set V_{LCD} range	0	0	0	0	0	0	0	1	0	PRS	V_{LCD} range L/H select
END	0	0	0	0	0	0	0	1	1	0	Release read/modify/write
Read/modify/write	0	0	0	0	0	0	0	1	1	1	RAM address at R:+0 , W:+1
Display control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
SI3-8bit data(L)&start	0	0	0	1	0	1	DA3	DA2	DA1	DA0	Specify the number of data bytes (8 bit 3-line SPI)
SI3-8bit data(L)	0	0	0	1	1	0	DA7	DA6	DA5	DA4	Specify the number of data bytes (8 bit 3-line SPI)
SI3-8bit data (M)	0	0	0	1	1	1	0	DA10	DA9	DA8	Specify the number of data bytes (8 bit 3-line SPI)
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	Sets Y address of RAM $0 \leqq Y \leqq 9$
Set Address (Low)	0	0	1	1	1	0	X3	X2	X1	X0	Set X address of RAM $0 \leqq X \leqq 131$
Set Address (High)	0	0	1	1	1	1	X7	X6	X5	X4	Set X address of RAM $0 \leqq X \leqq 131$
H[1:0]=[0:1]											
Display configuration	0	0	0	0	0	0	1	DO	0	V	Top/bottom row mode set data order
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Sets bias system (BSx)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V_{OP} to register

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
H[1:0]=[1:0]											
Partial screen mode	0	0	0	0	0	0	0	1	0	PS	Partial screen enable
Partial Display	0	0	0	0	0	0	1	0	0	WS	Set partial screen size
Partial Display part	0	0	0	0	0	1	DP3	DP2	DP1	DP0	Set display part for partial screen mode
Set Start line	0	0	1	S6	S5	S4	S3	S2	S1	S0	Specify the initial display line to realize vertical scrolling
H[1:0]=[1:1]											
RESET	0	0	0	0	0	0	0	0	1	1	Software reset
High Power Mode	0	0	1	0	1	1	0	HP	0	0	High Power Mode SET
Frame	0	0	0	0	0	0	1	FR2	FR1	FR0	Frame rate control
N line inversion	0	0	0	1	0	NL4	NL3	NL2	NL1	NL0	Sets N line inversion

n INSTRUCTION DESCRIPTION

H is independent

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Write data							

Read data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

Read status byte

Indicates the internal status of the ST7588

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	V	D	E	MX	MY	DO

Flag	Description		
PD	PD=0:chip is active PD=1:chip is in power down mode		
V	When V = 0, the horizontal addressing is selected. When V = 1, the vertical addressing is selected.		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	0	1	All display segments on
	1	0	Normal mode
	1	1	Inverse video mode
MX	SEG bi-direction selection MY=0:normal direction (SEG0(SEG131) MY=1:reverse direction (SEG131(SEG0)		
MY	COM bi-direction selection MY=0:normal direction (COM0(COM79) MY=1:reverse direction (COM79(COM0)		
DO	DO=0:MSB is on top DO=1:LSB is on top		

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MX	MY	PD	H1	H0

Flag	Description
MX	SEG bi-direction selection MY=0:normal direction (SEG0 **à** SEG131); MY=1:reverse direction (SEG131 **à** SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0 **à** COM79); MY=1:reverse direction (COM79 **à** COM0)
PD	All LCD outputs at V_{SS} (display off), bias generator and V_{LCD} generator off, V_{LCD} can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active; PD=1:chip is in power down mode
H0, H1	Selection of Extended Command Table

H[1:0]=[0:0]

Set V_{LCD} range

V_{LCD} range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0: VLCD programming range LOW

PRS=1: VLCD programming range HIGH

END

This command releases the read/modify/write mode, and returns the column and row address to the address it was at when the mode was entered.

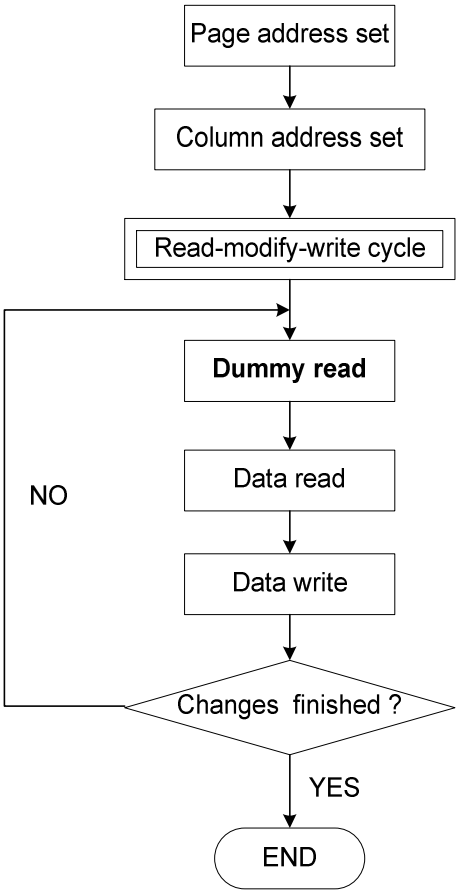
A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Read/modify/write

This command is used coupled with the “END” command. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is kept until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set SI3-8 bit Data

Display Data Length resister

This command is used in 8-bit 3-line SPI only. When A0 is not used, the Display Data Length instruction is used to indicate the specified number of display data byte to be transmitted. The next byte after the display data string is handled as command data.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	DA3	DA2	DA1	DA0
0	0	0	1	1	0	DA7	DA6	DA5	DA4
0	0	0	1	1	1	0	DA10	DA9	DA8

DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Display Data Length
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:	:	:	:
1	0	1	0	0	1	0	0	1	0	1	1317
1	0	1	0	0	1	0	0	1	1	0	1318
1	0	1	0	0	1	0	0	1	1	1	1319
1	0	1	0	0	1	0	1	0	0	0	1320

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 131
0	0	0	1	Page1 (display RAM)	0 to 131
0	0	1	0	Page2 (display RAM)	0 to 131
0	0	1	1	Page3 (display RAM)	0 to 131
0	1	0	0	Page4 (display RAM)	0 to 131
0	1	0	1	Page5 (display RAM)	0 to 131
0	1	1	0	Page6 (display RAM)	0 to 131
0	1	1	1	Page7 (display RAM)	0 to 131
1	0	0	0	Page8 (display RAM)	0 to 131
1	0	0	1	Page9 (display RAM)	0 to 131

Set X address of RAM

The X address points to the columns. The range of X is 0…131.

	A0	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
Set X Address (Low)	0	0	1	1	1	0	X3	X2	X1	X0
Set X address (High)	0	0	1	1	1	1	X7	X6	X5	X4

X7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column address
0	0	0	0	0	0		0	0
0	0	0	0	0	0		1	1
0	0	0	0	0	1		0	2
0	0	0	0	0	1		1	3
:	:	:	:	:	:		:	:
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

H[1:0]=[0:1]

Display configuration

Top/bottom row mode set data order and the direction of Address.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	DO	0	V

Flag	Description
DO	DO=0:MSB is on top DO=1:LSB is on top
V	When V = 0, the horizontal addressing is selected. When V = 1, the vertical addressing is selected.

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias	Recommend Duty
0	0	0	11	1/100
0	0	1	10	1/81
0	1	0	9	1/65, 1/68
0	1	1	8	1/49
1	0	0	7	1/40, 1/36
1	0	1	6	1/24
1	1	0	5	1/18, 1/16
1	1	1	4	1/10, 1/9, 1/8

LCD bias voltage

Symbol	Bias voltage for 1/9 bias	Symbol	Bias voltage for 1/9 bias
V_{LCD}	V_{LCD}	V3	2/9 X V_{LCD}
V1	8/9 X V_{LCD}	V4	1/9 X V_{LCD}
V2	7/9 X V_{LCD}	V_{SS}	V_{SS}

Set VOP value:

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

The operation voltage V_{LCD} can be set by software.

$$V_{LCD} = (a + V_{OP} \times b) \quad (1)$$

The parameters are described in table 4.The maximum voltage that can be generated is depending on the VDD1 voltage and the display load current. Two overlapping VLCD ranges are selectable via the command "Booster control". For the LOW (PRS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to "b" in both ranges. **Note that the charge pump is turned off if VOP [6;0] and the bit PRS are all set to zero.**

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	3.528(PRS=0)	V
a2	8.862(PRS=1)	V
b	0.042	V

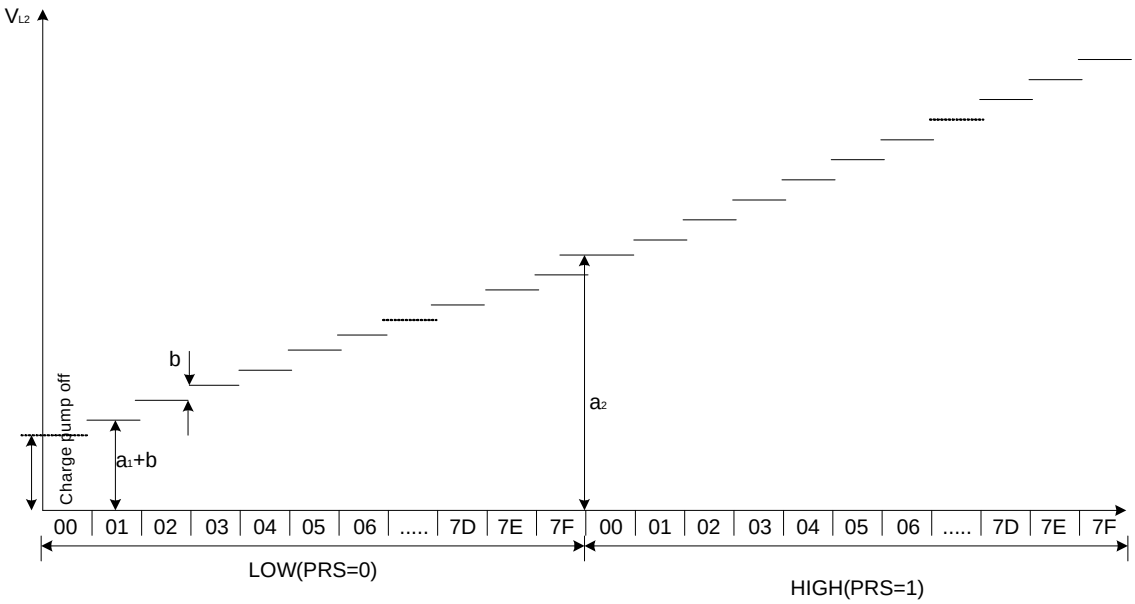


Fig.23 V_{OP} programming of ST7588

H[1:0]=[1:0]

Partial screen mode

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection PS=0:Full display mode with MUX 1:80 PS=1:Partial screen mode with MUX 1:16 or MUX 1:32

Partial screen size

This instruction can select partial screen size, partial screen 16 rows when WS is low and partial screen 32 rows when WS is high.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	WS

Display part

This instruction can select partial screen modes

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	DP3	DP2	DP1	DP0

1/16 Duty

Flag	Status				Description
DP3 DP2 DP1 DP0	0	0	0	0	RAM bank 0 to 1 (row0~row15)
	0	0	0	1	RAM bank 1 to 2 (row8~row23)
	0	0	1	0	RAM bank 2 to 3 (row16~row31)
	0	0	1	1	RAM bank 3 to 4 (row24~row39)
	0	1	0	0	RAM bank 4 to 5 (row32~row47)
	0	1	0	1	RAM bank 5 to 6 (row40~row55)
	0	1	1	0	RAM bank 6 to 7 (row48~row63)
	0	1	1	1	RAM bank 7 to 8 (row56~row71)
	1	0	0	0	RAM bank 8 to 9 (row64~row79)
	1	0	0	1	RAM bank 9 (row72~row79)

1/32 Duty

Flag	Status				Description
DP3 DP2 DP1 DP0	0	0	0	0	RAM bank 0 to 3 (row0~row31)
	0	0	0	1	RAM bank 1 to 4 (row8~row39)
	0	0	1	0	RAM bank 2 to 5 (row16~row47)
	0	0	1	1	RAM bank 3 to 6 (row24~row55)
	0	1	0	0	RAM bank 4 to 7 (row32~row63)
	0	1	0	1	RAM bank 5 to 8 (row40~row71)
	0	1	1	0	RAM bank 6 to 9 (row48~row79)
	0	1	1	1	RAM bank 7 to 9 (row56~row79)
	1	0	0	0	RAM bank 8 to 9 (row64~row79)
	1	0	0	1	RAM bank 9 (row72~row79)

Set start line

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	S6	S_5	S_4	S_3	S_2	S_1	S_0

S_6	S_5	S_4	S_3	S_2	S_1	S_0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	0	0	1	1	0	1	77
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

Note: when 81duty is selected, 4f (1001111) is MAX;
when 65 duty is selected, 3f (0111111) is MAX;
when 49 duty is selected, 2f (0101111) is MAX

H[1:0]=[1:1]

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status .This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

High Power Mode

This command is to enter the high power mode. HP=1: high power mode, HP=0: normal mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	HP	0	0

Frame frequency

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FR2	FR1	FR0

This command is used to set the frame frequency.

FR_2	FR_1	FR_0	Frame frequency
0	0	0	60 Hz ±5%
0	0	1	70 Hz ±5%
0	1	0	75 Hz ±5%
0	1	1	80 Hz ±5%
1	0	0	83 Hz ±5%
1	0	1	86 Hz ±5%
1	1	0	90 Hz ±5%
1	1	1	165 Hz ±5%

Set N-line inversion

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M)

Note: The N-line inversion mode will be disabled when partial display mode enter. After the partial display mode end, the N-line inversion mode will return as it was.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	NL4	NL3	NL2	NL1	NL0

NL4	NL3	NL2	NL1	NL0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

n COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

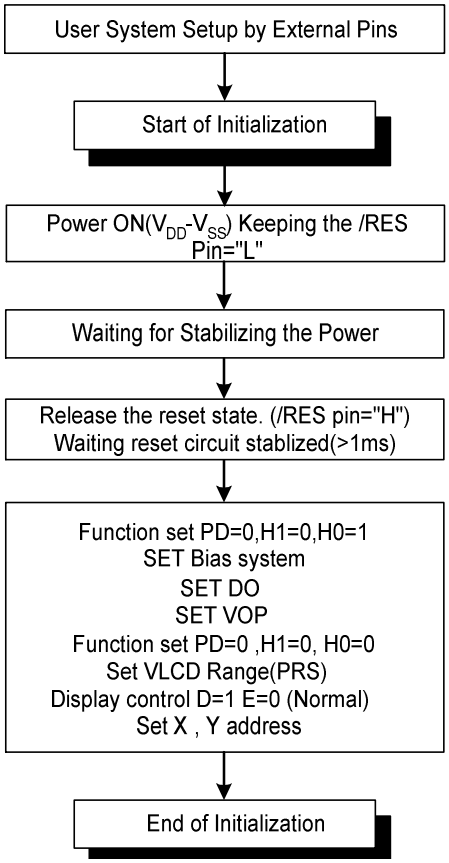


Fig.24 Initializing with the Built-in Power Supply Circuits

Referential Instruction Flow for Power Down:

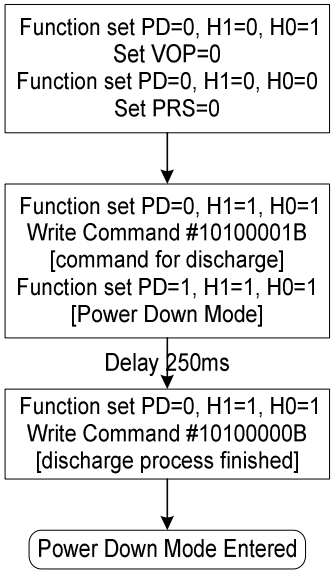
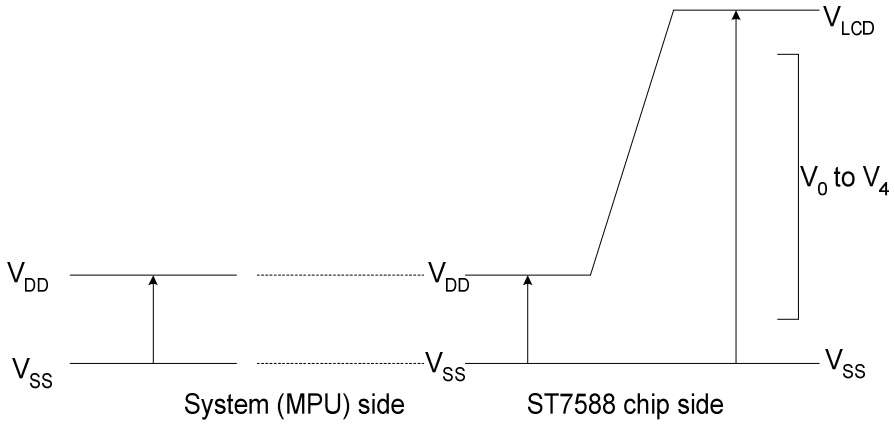


Fig.25 Instruction Flow for Power Down

n LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	V_{DD1}	1.3 ~ 3.7	V
Power supply voltage	V_{DD2}	1.3 ~ 3.7	V
Power supply voltage (V_{DD} standard)	VOUT	–0.5 ~ +15	V
Power supply voltage (V_{DD} standard)	V1, V2, V3, V4	0.3 to V0	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature	TOPR	–40 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   VOUT ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

n DC CHARACTERISTICS

V_{DD} = 1.8 V to 3.3V; V_{SS} = 0 V; V_{LCD} = 4.5 to 14.0V; T_{amb} = -40℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		V_{DD1}			1.8	--	3.3	V	V_{SS}
Operating Voltage (2)		V_{DD2}	(Relative to V_{SS})		1.8	--	3.3	V	V_{SS}
High-level Input Voltage		V_{IHC}			0.7 x V_{DD}	--	V_{DD}	V	
Low-level Input Voltage		V_{ILC}			V_{SS}	--	0.3 x V_{DD}	V	
High-level Output Voltage		V_{OHC}	I_{OH}=1mA		0.7 x V_{DD}	--	V_{DD}	V	
Low-level Output Voltage		V_{OLC}	I_{OL}=1mA		V_{SS}	--	0.3 x V_{DD}	V	
Input leakage current		I_{LI}	VIN = V_{DD} or V_{SS}		-1.0	--	1.0	µA	
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{SS})	V_{LCD} = 11.0 V	--	0.8	1.1	kΩ	SEGn COMn
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/81 duty		--	53	--	kHz	*1
	Frame frequency	f_{FRAME}			--	80	--	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	V_{DD}	(Relative To V_{SS})	1.8	--	3.3	V	V_{SS}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative To V_{SS})	--	--	15.0	V	V_{SS}, *2

Dynamic Consumption Current: During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	I_{SS}	V_{DD} = 3.0 V, V0 – V_{SS} = 10.0 V	--	120	--	µA	*3
Power Down	I_{SS}	Ta = 25°C	--	0.05	2	µA	*4

Notes to the DC characteristics

1. Internal clock
2. The maximum possible V_{OUT} voltage that may be generated is dependent on voltage, temperature and (display) load.
3. If external V_{LCD} used, the display load current is not transmitted to I_{DD}.
4. Power-down mode. During power down all static currents are switched off.

n TIMING CHARACTERISTICS

I System Bus Read/Write Characteristics(For the 8080 Series MPU)

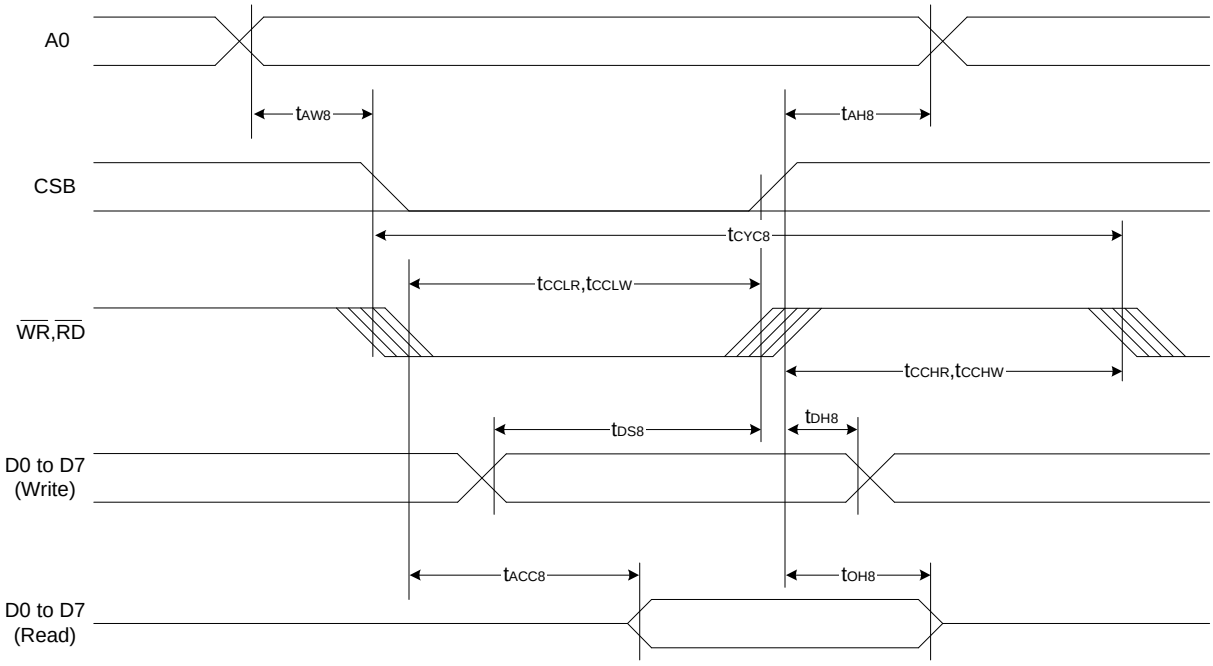


Figure 26

(V_{DD} = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		80	--	
Enable L pulse width (WRITE)	WR	t_{CCLW}		70	--	
Enable H pulse width (WRITE)		t_{CCHW}		30	--	
Enable L pulse width (READ)	RD	t_{CCLR}		90	--	
Enable H pulse width (READ)		t_{CCHR}		30	--	
WRITE Data setup time	D0 to D7	t_{DS8}		80	--	
WRITE Data hold time		t_{DH8}		20	--	
READ access time		t_{ACC8}	C_L = 100 pF	--	50	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	30	

(V_{DD} = 2.7 V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		90	--	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	--	
Enable H pulse width (WRITE)		t_{CCHW}		30	--	
Enable L pulse width (READ)	RD	t_{CCLR}		110	--	
Enable H pulse width (READ)		t_{CCHR}		30	--	
WRITE Data setup time	D0 to D7	t_{DS8}		90	--	
WRITE Data hold time		t_{DH8}		20	--	
READ access time		t_{ACC8}	C_L = 100 pF	--	60	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	40	

(V_{DD} = 1.8V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		220	--	
Enable L pulse width (WRITE)	WR	t_{CCLW}		200	--	
Enable H pulse width (WRITE)		t_{CCHW}		30	--	
Enable L pulse width (READ)	RD	t_{CCLR}		220	--	
Enable H pulse width (READ)		t_{CCHR}		30	--	
WRITE Data setup time	D0 to D7	t_{DS8}		220	--	
WRITE Data hold time		t_{DH8}		20	--	
READ access time		t_{ACC8}	C_L = 100 pF	--	100	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	30	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

I System Bus Read/Write Characteristics(For the 6800 Series MPU)

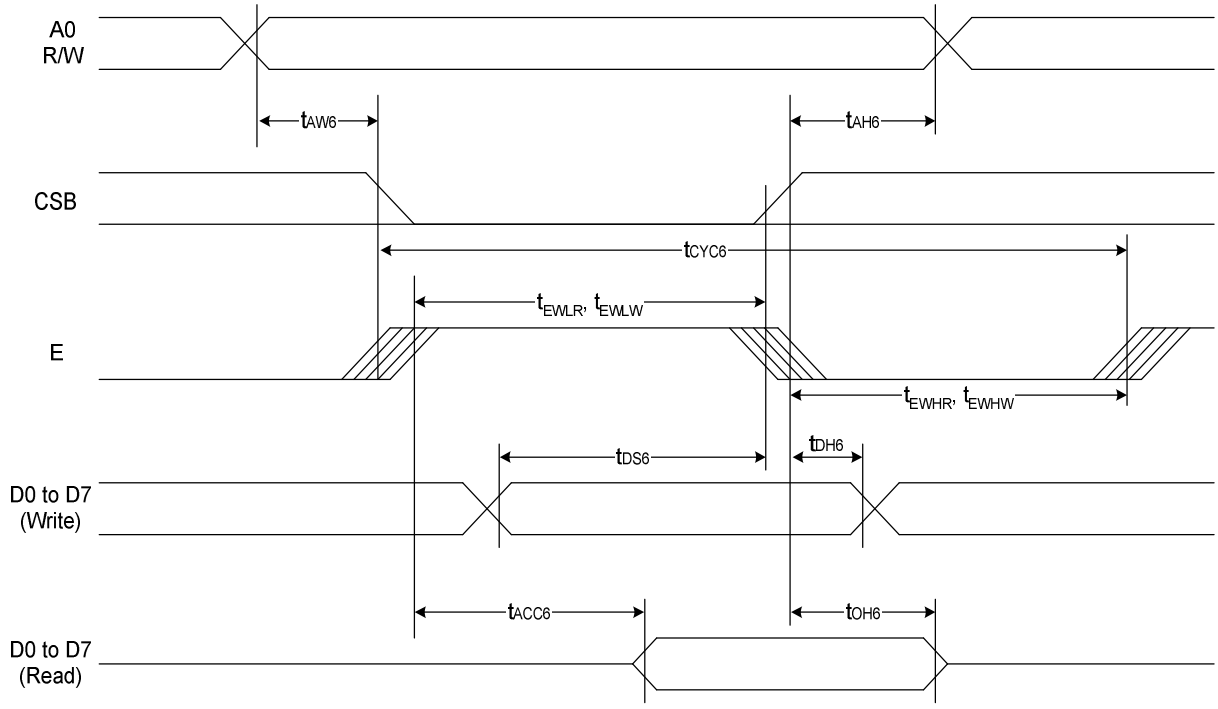


Figure 17

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		60	--	
System cycle time		t_{CYC6}		100	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		30	--	
Enable H pulse width (WRITE)		t_{EWHW}		40	--	
Enable L pulse width (READ)	RD	t_{EWLR}		30	--	
Enable H pulse width (READ)		t_{EWHR}		40	--	
WRITE Data setup time	D0 to D7	t_{DS6}		70	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

(V_{DD} = 2.7V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		70	--	
System cycle time		t_{CYC6}		140	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		30	--	
Enable H pulse width (WRITE)		t_{EWHW}		40	--	
Enable L pulse width (READ)	RD	t_{EWLR}		30	--	
Enable H pulse width (READ)		t_{EWHR}		40	--	
WRITE Data setup time	D0 to D7	t_{DS6}		90	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	80	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

(V_{DD} =1.8V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		80	--	
System cycle time		t_{CYC6}		270	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		40	--	
Enable H pulse width (WRITE)		t_{EWHW}		60	--	
Enable L pulse width (READ)	RD	t_{EWLR}		40	--	
Enable H pulse width (READ)		t_{EWHR}		70	--	
WRITE Data setup time	D0 to D7	t_{DS6}		210	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	80	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

I SERIAL INTERFACE (IIC Interface)

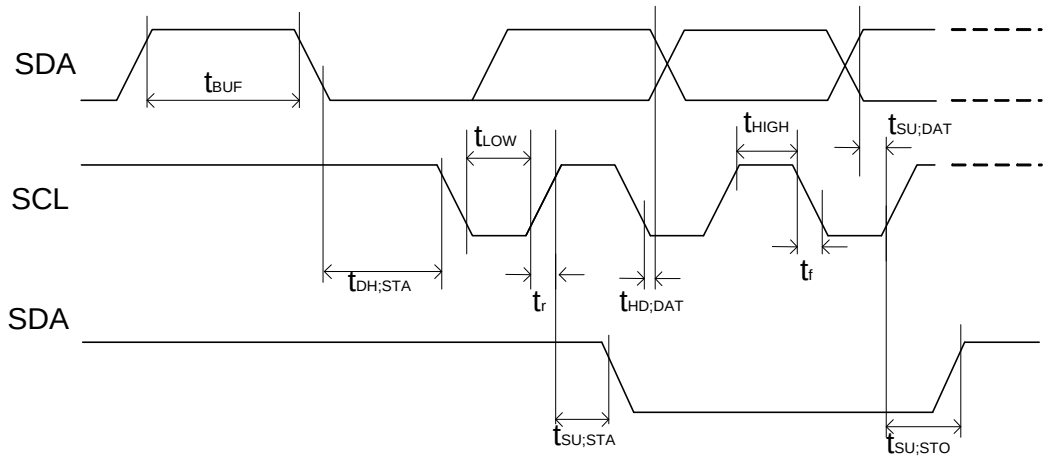


Figure 18

(V_{DD}=3.3V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}		DC	400	kHz
SCL clock low period	SCL	t_{LOW}		150	--	ns
SCL clock high period	SCL	t_{HIGH}		100	--	
Data set-up time	SDA	$t_{SU;Dat}$		90	--	
Data hold time	SDA	$t_{HD;Dat}$		40	--	
Setup time for a repeated START condition	SDA	$t_{SU;STA}$		70	--	
Start condition hold time	SDA	$t_{HD;STA}$		170	--	
Setup time for STOP condition		$t_{SU;STO}$		90	--	
BUS free time between a STOP and START condition	SCL	t_{BUF}		70	--	

(V_{DD}=2.7V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}		DC	400	kHz
SCL clock low period	SCL	t_{LOW}		190	--	ns
SCL clock high period	SCL	t_{HIGH}		110	--	
Data set-up time	SDA	$t_{SU;Dat}$		110	--	
Data hold time	SDA	$t_{HD;Dat}$		30	--	
Setup time for a repeated START condition	SDA	$t_{SU;STA}$		90	--	
Start condition hold time	SDA	$t_{HD;STA}$		220	--	
Setup time for STOP condition		$t_{SU;STO}$		110	--	
BUS free time between a STOP and START condition	SCL	t_{BUF}		90	--	

(V_{DD}=1.8V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}		DC	400	kHz
SCL clock low period	SCL	t_{LOW}		500	--	ns
SCL clock high period	SCL	t_{HIGH}		250	--	
Data set-up time	SDA	$t_{SU;Dat}$		270	--	
Data hold time	SDA	$t_{HD;Dat}$		80	--	
Setup time for a repeated START condition	SDA	$t_{SU;STA}$		230	--	
Start condition hold time	SDA	$t_{HD;STA}$		480	--	
Setup time for STOP condition		$t_{SU;STO}$		270	--	
BUS free time between a STOP and START condition	SCL	t_{BUF}		210	--	

I SERIAL INTERFACE (4-Line Interface)

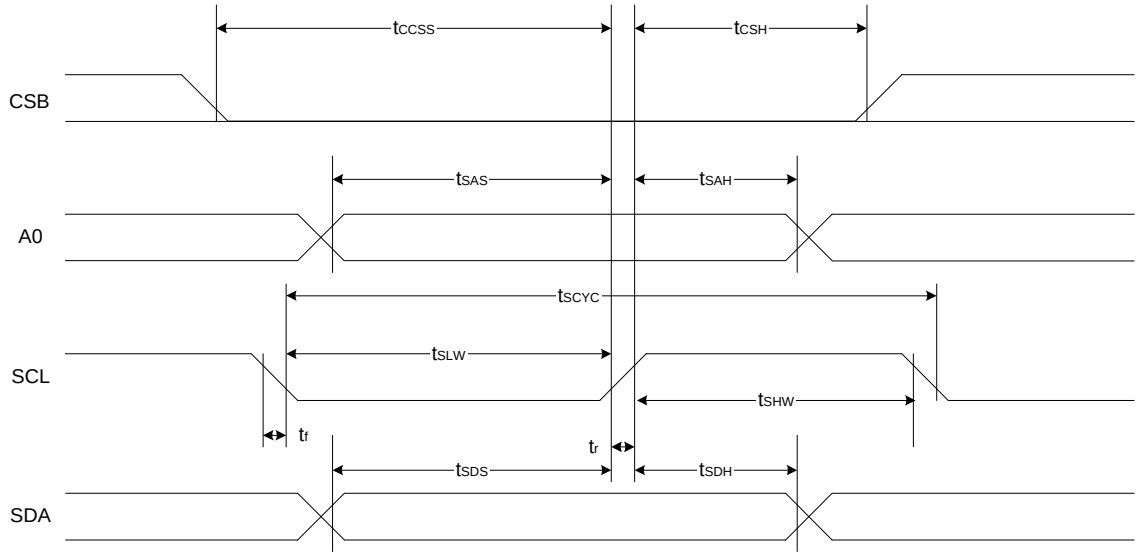


Figure 19

(V_{DD}=3.3V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	--	ns
SCL “H” pulse width		t_{SHW}		60	--	
SCL “L” pulse width		t_{SLW}		60	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		80	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		120	--	

(V_{DD}=2.7V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		120	--	ns
SCL “H” pulse width		t_{SHW}		70	--	
SCL “L” pulse width		t_{SLW}		70	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		100	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		150	--	

(V_{DD}=1.8V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330	--	ns
SCL “H” pulse width		t_{SHW}		150	--	
SCL “L” pulse width		t_{SLW}		150	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		160	--	
Data setup time	SDA	t_{SDS}		40	--	
Data hold time		t_{SDH}		40	--	
CS-SCL time	CSB	t_{CSS}		40	--	
CS-SCL time		t_{CSH}		370	--	

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

I SERIAL INTERFACE (3-Line Interface)

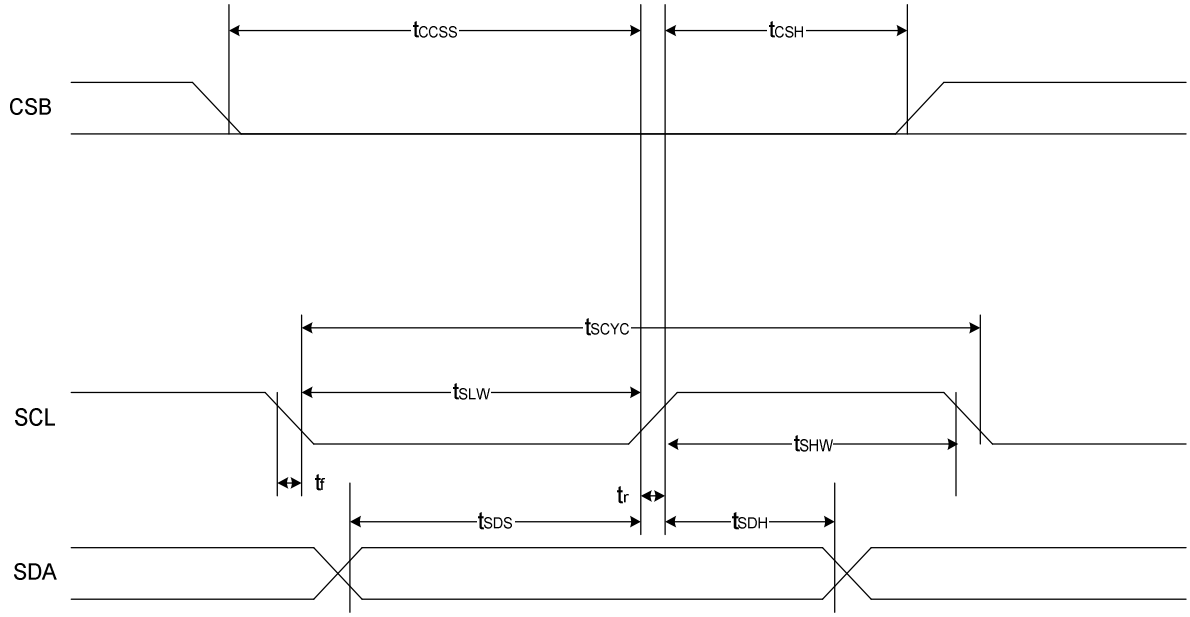


Figure 20

(V_{DD}=3.3V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	--	ns
SCL “H” pulse width		t_{SHW}		60	--	
SCL “L” pulse width		t_{SLW}		60	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		120	--	

(V_{DD}=2.7V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		120	--	ns
SCL “H” pulse width		t_{SHW}		70	--	
SCL “L” pulse width		t_{SLW}		70	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		150	--	

(V_{DD}=1.8V, Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330	--	ns
SCL “H” pulse width		t_{SHW}		150	--	
SCL “L” pulse width		t_{SLW}		150	--	
Data setup time	SDA	t_{SDS}		40	--	
Data hold time		t_{SDH}		40	--	
CS-SCL time	CSB	t_{CSS}		40	--	
CS-SCL time		t_{CSH}		370	--	

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

n RESET TIMING

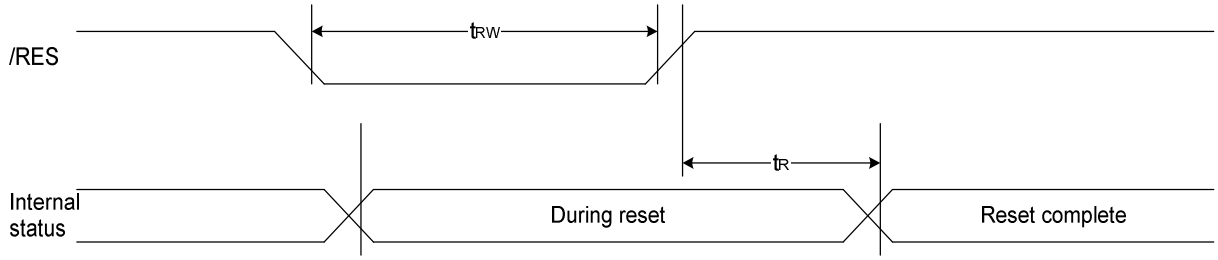


Figure 21

(V_{DD} = 3.3V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	400	ns
Reset “L” pulse width	/RES	t_{RW}		1.2	--	--	µs

(V_{DD} = 2.7V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	350	ns
Reset “L” pulse width	/RES	t_{RW}		1.6	--	--	µs

(V_{DD} = 1.8V, Ta = –40 to 85°C)

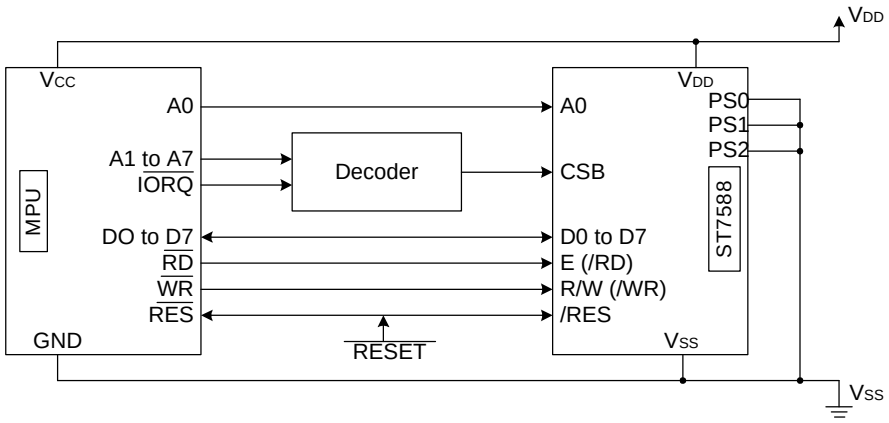
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	140	ns
Reset “L” pulse width	/RES	t_{RW}		4.5	--	--	µs

THE MPU INTERFACE (REFERENCE EXAMPLES)

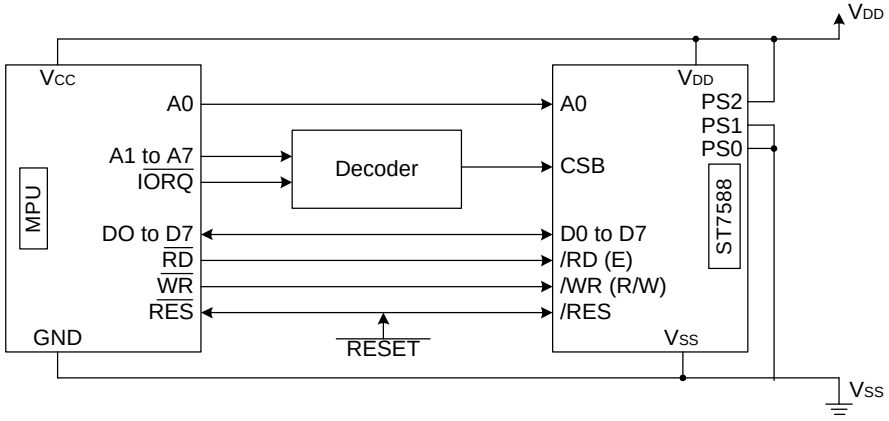
The ST7588 Series can be connected to either 80X86 Series MPU or to 6800 Series MPU. Moreover, using the serial interface it is possible to operate the ST7588 series chips with fewer signal lines.

The display area may be expanded by using multiple ST7588 Series chips. In this application, the chip select signal can be used to select the individual ICs to access.

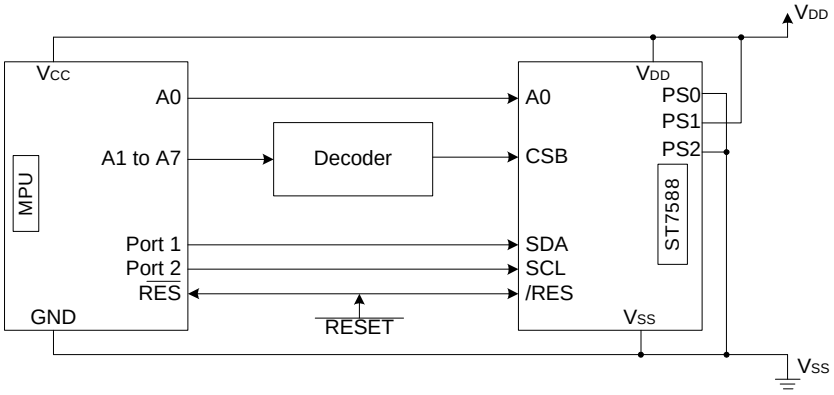
(1) 8080 Series MPU



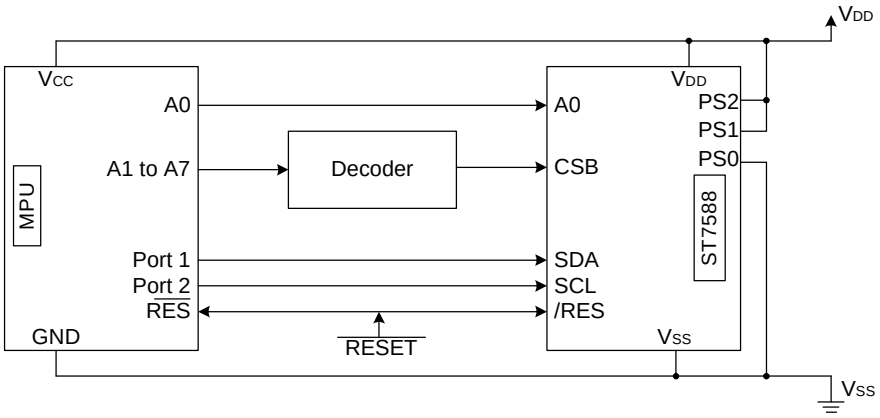
(2) 6800 Series MPU



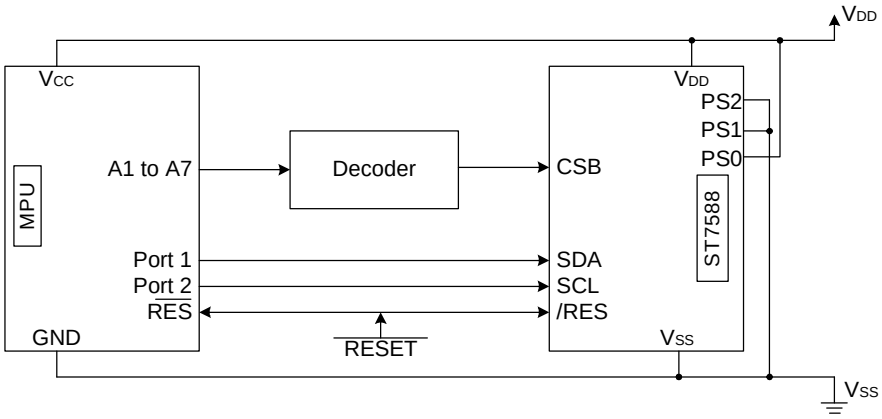
(3) Using the Serial Interface (4-line interface A mode)



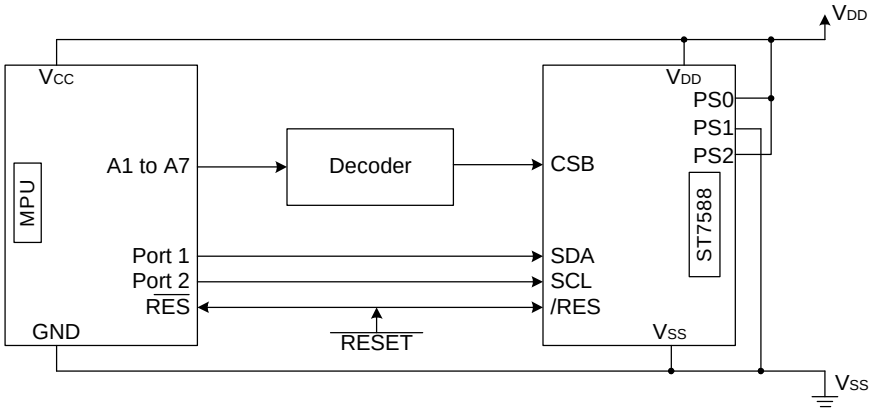
(4) Using the Serial Interface (4-line interface B mode)



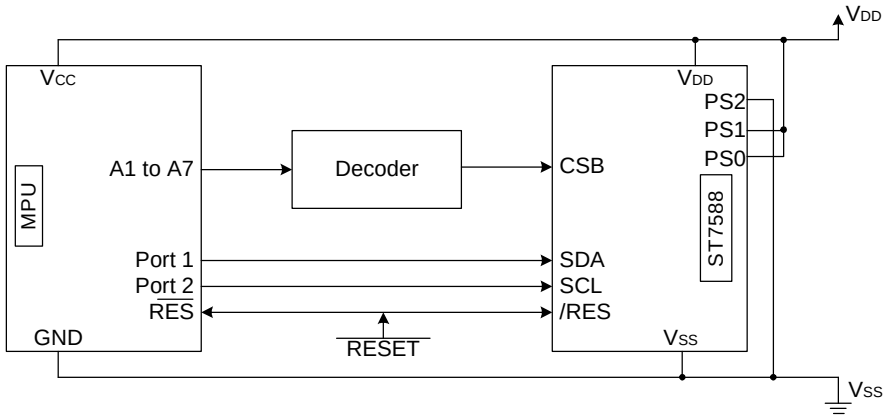
(5) Using the Serial Interface (3-line interface 8 bit A mode)



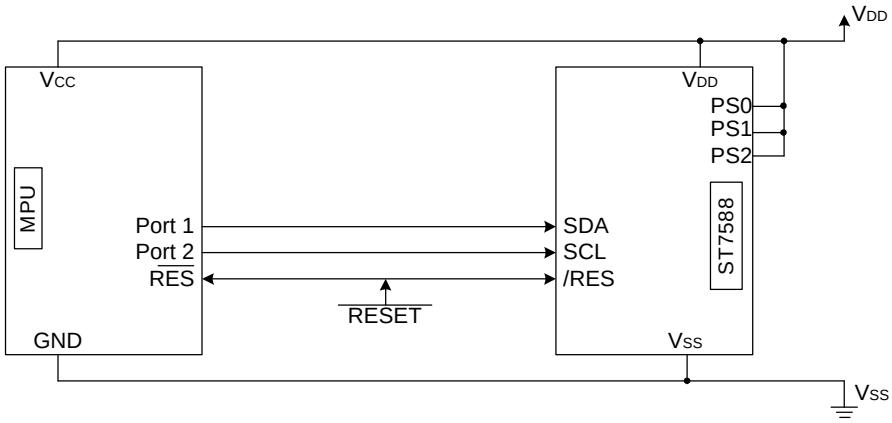
(6) Using the Serial Interface (3-line interface 8 bit B mode)



(7) Using the Serial Interface (3-line interface 9 bit)

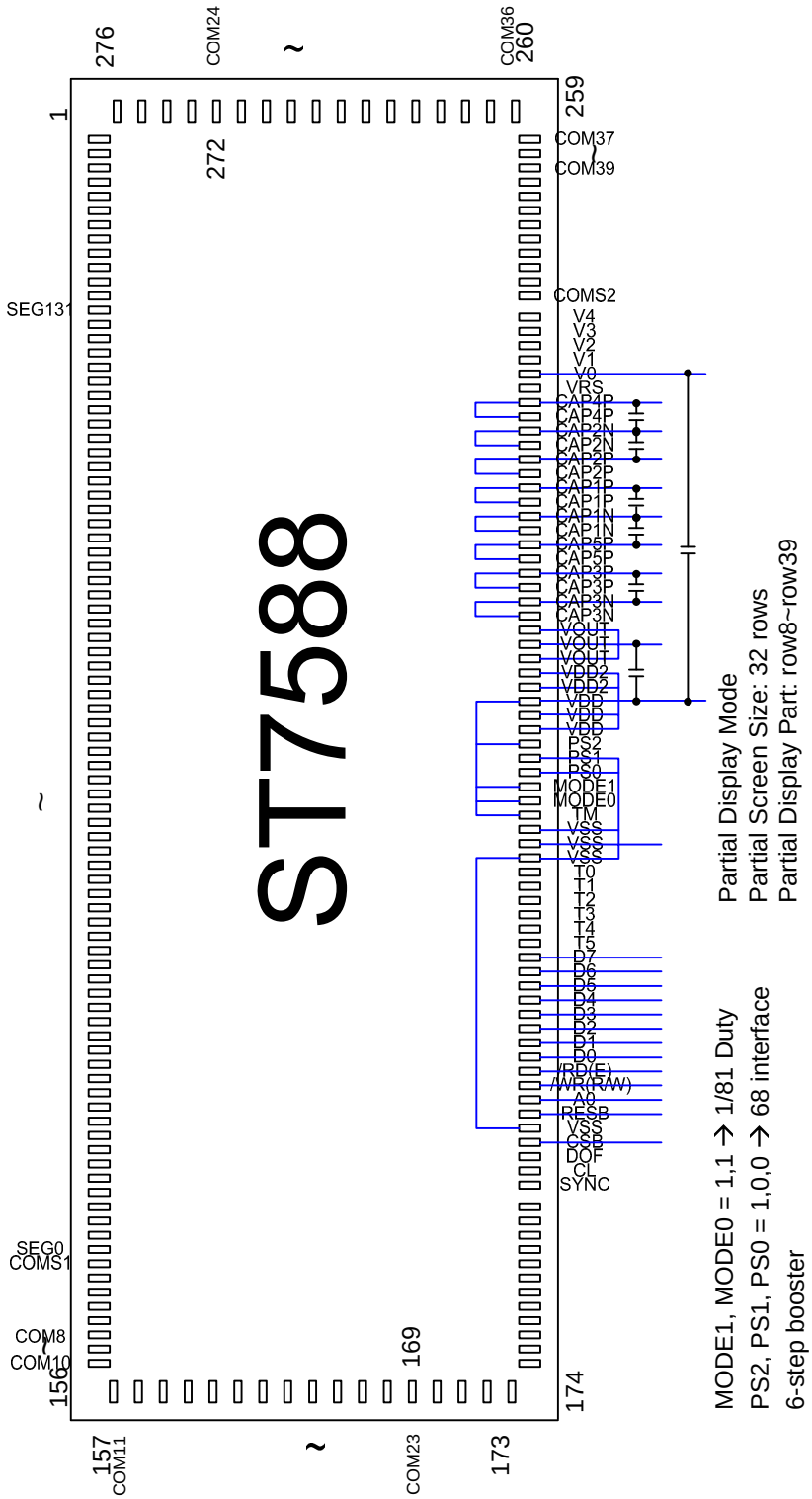


(8) Using the Serial Interface (I^2C interface)

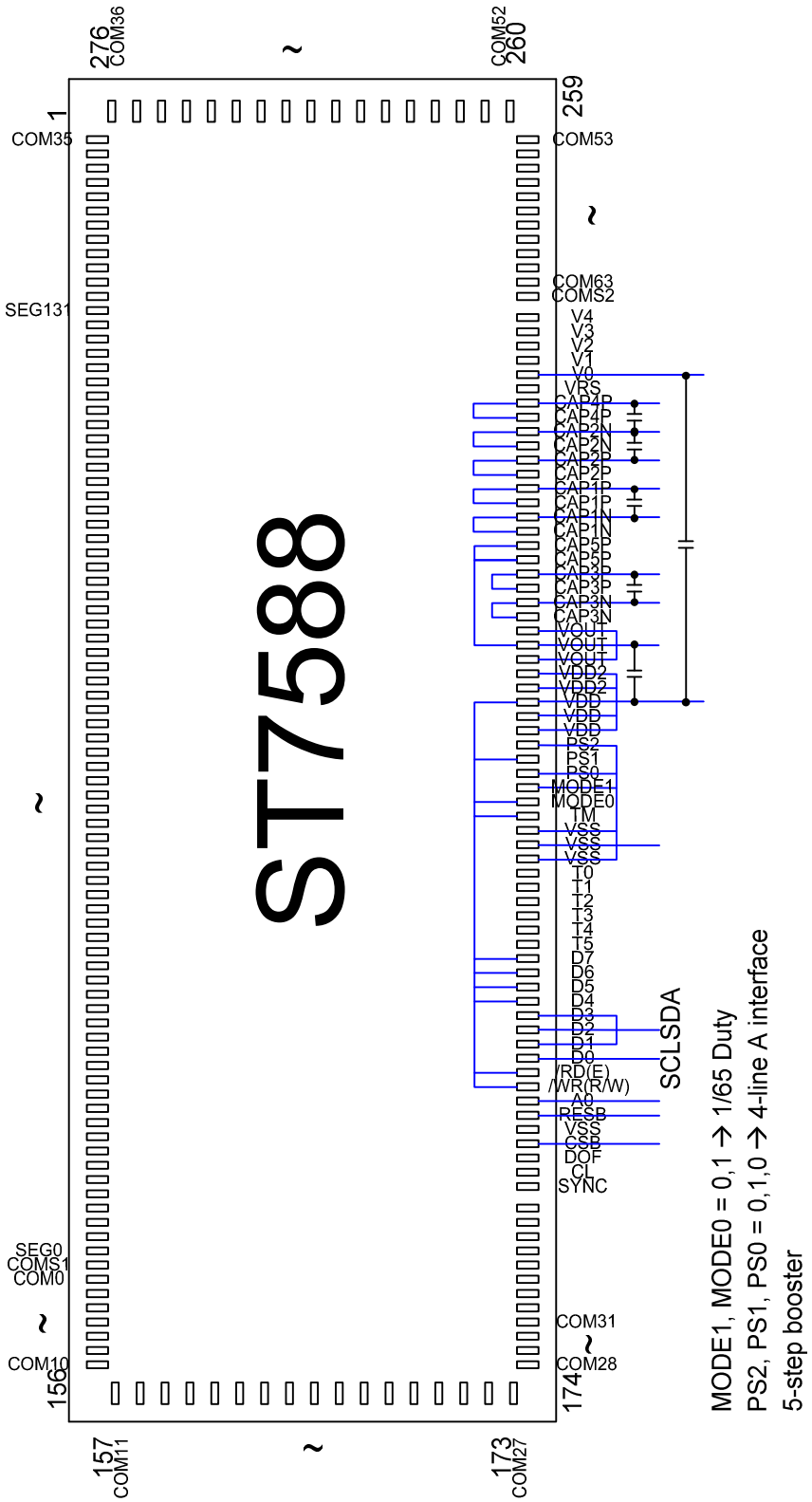


n APPLICATION CIRCUITS

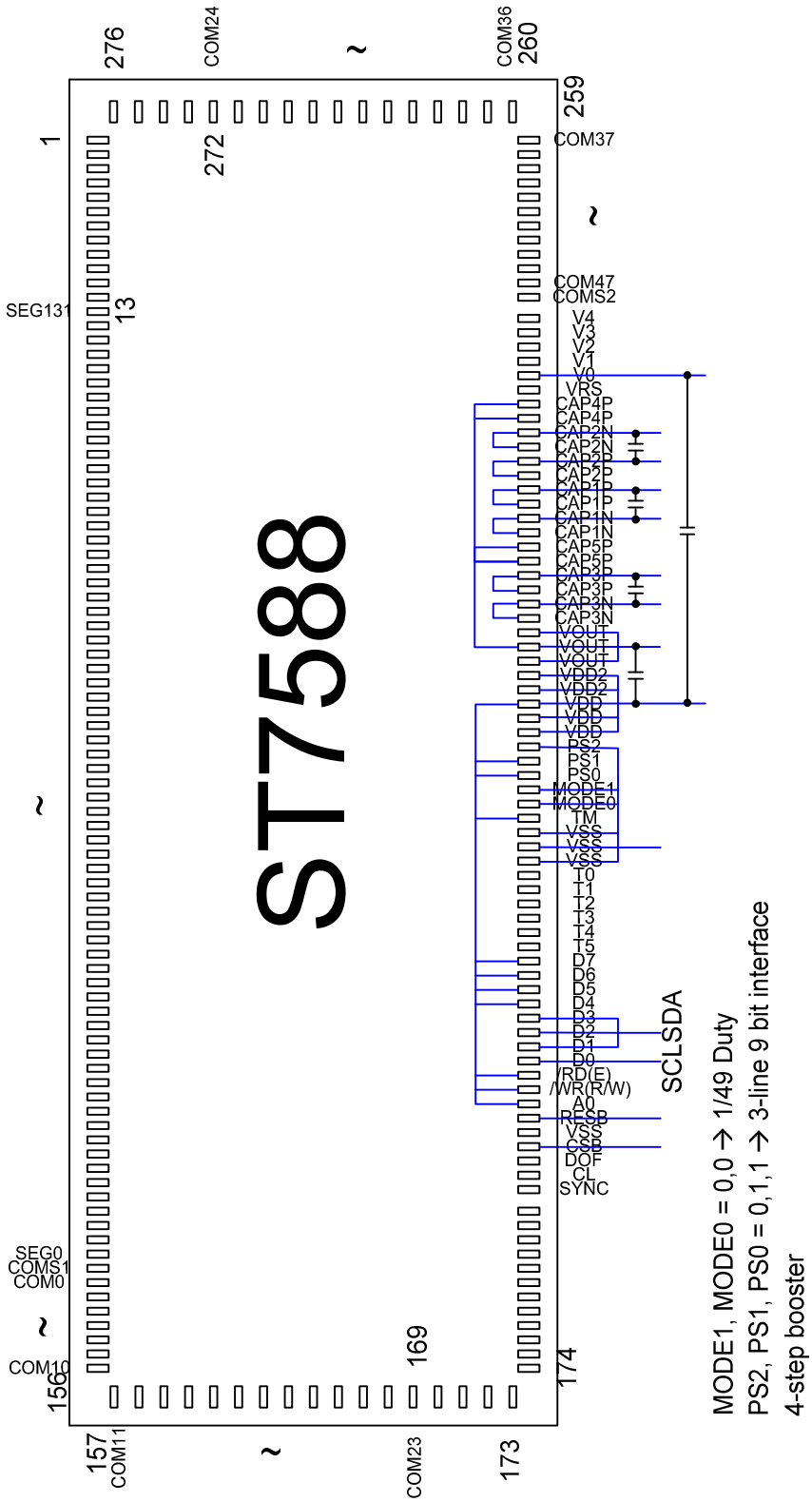
For the 6800 interface & 32 duty (partial display)



For the 4-line A interface & 65 duty

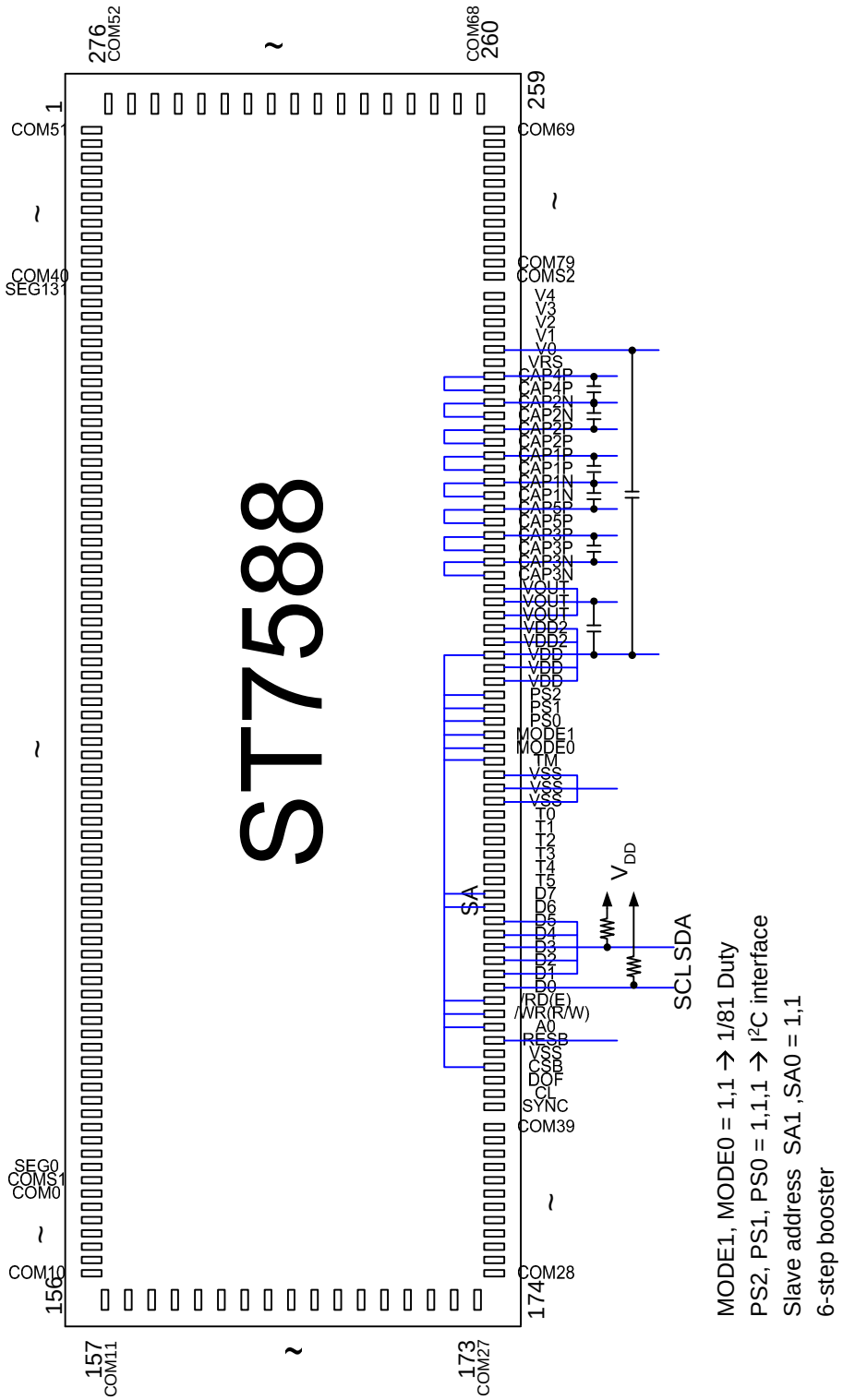


For the 3-line 9 bit interface & 49 duty



For the I²C interface & 81 duty

In I²C application, note that the impedence of SDAs and GNDs should be keep in the POWER PIN LEVEL.



Change Note:

0.2 version Page 21 cap connection

0.3 syntax correction

0.4 The PS[2:0] description

Cap connection of booster

description of partial display command

Pin assignment of I^2C interface

Frame range

Instruction table

0.5 chip size

Change FR as SYNC

The writing data flow of 3-line A and 3-line B interface

Vop value

Remove reserved command

0.6 add application circuit

More detailed Pad Center Coordinates

0.7 bump height

The PS[2:0] description

Pin descriptions

Serial Interface description

The MPU interface reference examples

Chip size

0.8 Vop value

Timing characteristics

DC characteristics

Limiting values

Application circuit

Instruction Flow for Power Down

Release [high power mode] command

I^2C interface notification

0.9 ITO Limitations

Application circuit

1.0 remove preliminary

remove master-slave function

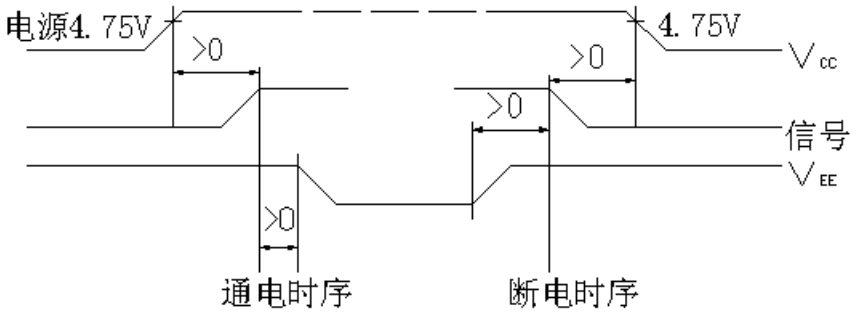
I^2C SCL clock frequency

1.1 Chip Thickness

Application circuit

液晶显示模块使用注意事项

1. 请勿随意自行加工、整修、拆卸。
2. 避免对液晶屏表面施加压力。
3. 不要用手随意去摸外引线、电路板上的电路及金属框。
4. 如必须直接接触时，应使人体与模块保持同一电位，或将人体良好接地。
5. 焊接使用的烙铁、操作用的电动改锥等工具必须良好接地，没漏电。
6. 严防各种静电。
7. 模块使用接入电源及断开电源时，必须按图时序进行。即必须在正电源（ 5 ±0.25V）稳定接入后,才能输入信号电平。如在电源稳定接入前，或断开后就输入信号电平，将会损坏模块中的集成电路，使模块损坏。



8. 点阵模块在调节时，应调整 VEE 至最佳对比度、视角时为止。如果 VEE 调整过高,不仅会影响显示，还会缩短液晶的寿命。
9. 模块表面结雾时，不要通电工作，因为这将引起电极化学反应，产生断线。
10. 模块要存储在暗处（避阳光），温度在-10℃～+35℃，湿度在 RH60%以上的地方。如能装入聚乙烯口袋（最好有防静电涂层）并将口封住最好。

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